 By Jeff Ju, Fairchild Semiconductor

UNDERSTANDING THE ELECTRICAL CHARACTERISTICS AND TERMINATION REQUIREMENTS FOR BEST OPERATION IS CRITICAL FOR A SUCCESSFUL DESIGN AND, ULTIMATELY, A RELIABLE INTERFACE.

Interfacing LVDS with other differential-I/O types

Interface design is one of the most critical considerations affecting high-performance data transfer. The interoperability of each I/O presents challenges that often impact design cycles and time to market. In high-speed-system design, differential I/O, such as LVDS (low-voltage differential signaling), LVPECL (low-voltage positive emitter-coupled logic), and CML (current-mode logic) have become increasingly popular due to their ability to tolerate common-mode noise. However, transitioning between disparate I/O types can be problematic if you fail to consider their technological differences.

LVDS CHARACTERISTICS

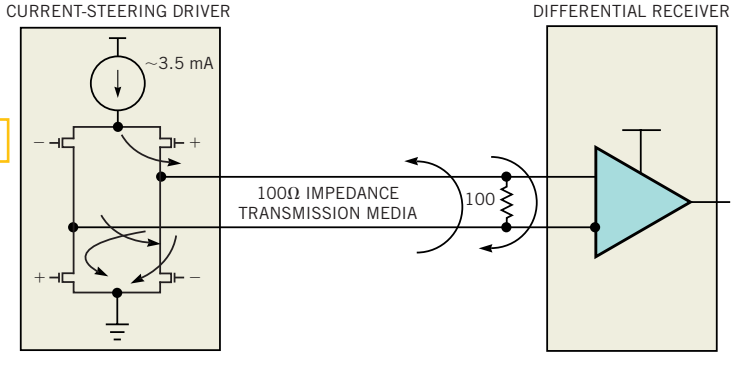
The ANSI/TIA/EIA-644 standard defines LVDS I/O as a low-voltage, low-power, differential technology primarily targeting point-to-point data communications. The standard, developed under the TR30.2 Data Transmission Interface Committee, specifies a maximum data rate of 655 Mbps—although some of today's serial data-stream transfer rates exceed this specification. Compared with other differential cable-driving standards, such as RS-422 and RS-485, LVDS has the lowest differential voltage swing—typically 350 mV with an offset of 1.2V above ground. The simplified reference circuit in **Figure 1** illustrates the point-to-point link.

LVDS provides a balanced current source output, in which positive and negative signals 180° apart create the differential voltage. The receiver detects the differential voltage to interpret the logic. A 100Ω resistor provides the differential termination matching the differential impedance of the transmission lines for optimum signal integrity. A typical LVDS receiver can interface with other differential technologies, provided that the signal levels are within the common-mode range of 0 to 2.4V. **Table 1** summarizes the specification limits for six key LVDS parameters.

LVPECL CHARACTERISTICS

LVPECL features emitter-follower output stages. By terminating a 50Ω resistor to V_{CC} − 2V, you ensure that 14 mA of dc current is always flowing through the emitter of the output transistors. This constant current flow enables the LVPECL output to rapidly change states. In addition, the emitter-follower stage has very low output impedance and can thus efficiently maintain the unity gain. The temperature-compensated output buffer of a typical 100 Series LVPECL provides a stable output swing over both process and temperature. One of the most important features of LVPECL is that it common-mode references its output to V_{CC} instead of ground. **Figure 2** illustrates an LVPECL reference circuit with

Figure 1



The simplified reference circuit conceptualizes one LVDS differential pair.

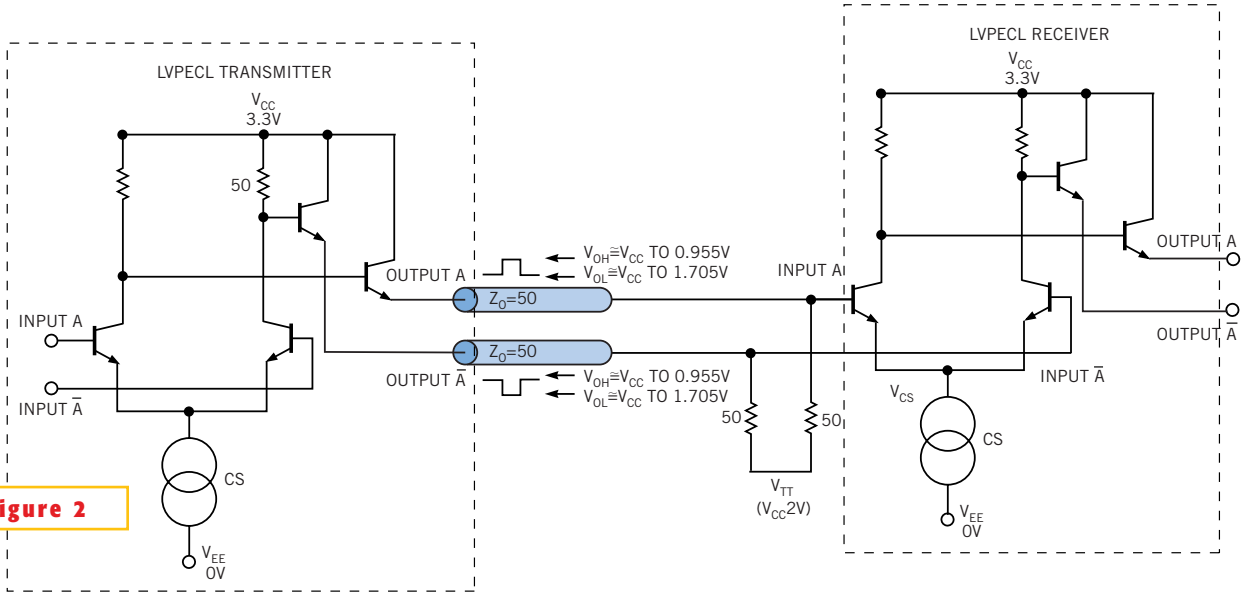


Figure 2

LVPECL buffers typically have this architecture.

the appropriate termination for normal operation. **Table 2** summarizes the specification limits for seven key LVPECL parameters.

CML CHARACTERISTICS

CML provides a current-switching output buffer (**Figure 3**). You typically source-terminate CML drivers to V_{CC} with a 50Ω resistor for optimal signal integrity. The common-mode voltage of the CML driver output can be either V_{CC} or ground-based, but it typically refers to V_{CC} with an offset voltage of about $V_{CC}-0.2V$, which is higher than both the LVDS and the LVPECL drivers. At the receiver side, it typically offers a 50Ω far-end termination to provide a 400-mV swing at the driver side. You can build far-end termination inside the receivers. **Table 3** includes important dc characteristics of both CML drivers and receivers.

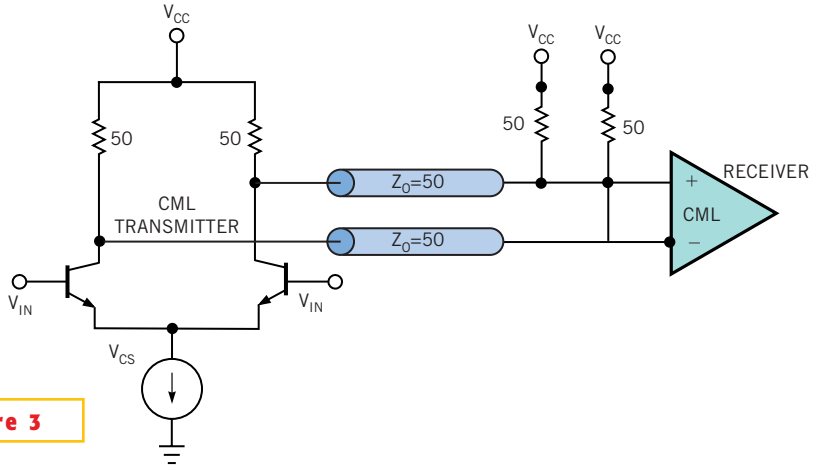


Figure 3

CML provides a current-switching output buffer.

INTERFACING DIFFERENTIAL LOGIC

Engineers can extend the two ways of interfacing between LVDS, LVPECL, and CML—the dc coupling method and ac coupling method—to the interface with TMDS (transition-minimized differential signaling) and other differential logic.

The dc-coupling method is based on a dc-shift-resistor network. Depending on the common-mode range relationship between the driver and the receiver, you can step up or step down the common-mode voltage. Designers generally use the Thevenin-resistor network-analysis method for interconnecting with dc coupling.

Figure 4 shows an example of how LVPECL drivers "talk" to LVDS receivers. Because the LVPECL has a higher common-mode voltage than the LVDS, you insert a step-down resistor network to reduce the common-mode voltage from $V_{CC}-1.3V$ to 1.2V. Some manufacturers' LVDS receivers provide internal termination resistors, and others do not.

When selecting resistor values, engineers must: Make sure that the Thevenin

TABLE 1–TYPICAL CHARACTERISTICS OF LVDS INPUT AND OUTPUT*

Transmitter with LVDS output					Receiver with LVDS input				
Parameter	Symbol	Minimum	Typical	Maximum	Parameter	Symbol	Minimum	Typical	Maximum
Output high (V)	V_{OH}	1.249	1.375	1.602	Input common-mode yange	V_I	0.5		2.35
Output low (V)	V_{OL}	1.002	1.025	1.148	Threshold	V_{TH}	0.1		
Differential output voltage (V)	V_{OD}	0.247	0.350	0.454					
Offset voltage (V)	V_{CM}	1.125	1.2	1.375					

*V_{CC}=3.3V ± 10V.

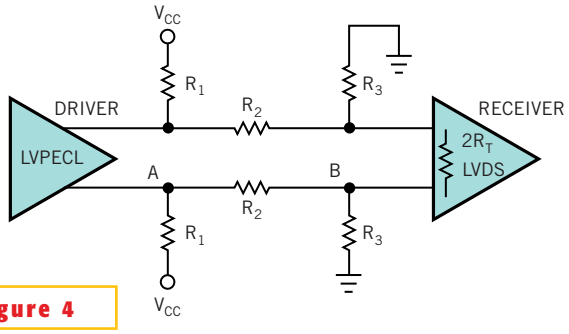


Figure 4

A step-down resistor network provides the interface between LVPECL drivers and LVDS receivers.

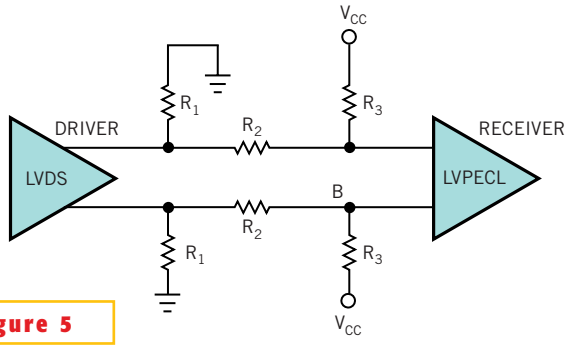


Figure 5

A step-up resistor network interfaces LVDS drivers to LVPECL receivers.

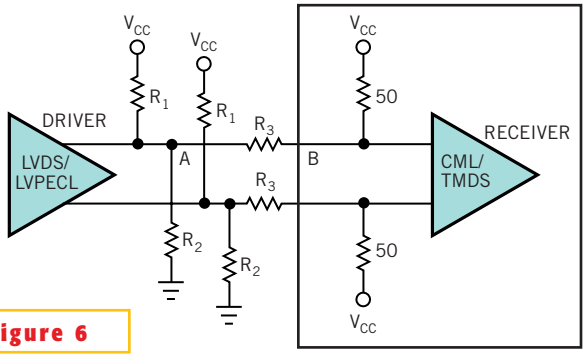


Figure 6

A typical architecture shows how LVDS/LVPECL drivers and CML/TMDS receivers communicate with each other.

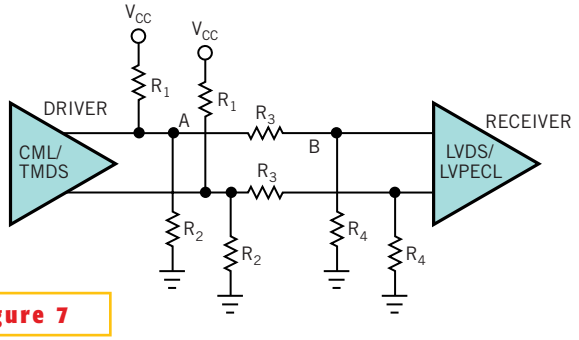


Figure 7

A typical architecture shows how CML/TMDS drivers and LVDS/LVPECL receivers "talk" to each other.

voltage at Node A equals the termination voltage ($V_{CC}-2V$):

$$V_A = \frac{R_2 + R_3}{R_1 + R_2 + R_3} = V_{CC} - 2.$$

They must also ensure that the equivalent Thevenin impedance at Node A is 50Ω:

$$R_{AC} = R_1 \| (R_2 + R_3) = 50$$

for receivers with no internal termination, and

$$R_{AC} = R_1 \| (R_2 + (R_3 \| R_T)) = 50$$

for receivers with internal termination resistor, R_T (45 to 66Ω).

The Thevenin voltage at node B should be sitting on the "sweet spot" of the LVDS receiver (1.2V):

$$V_B = \frac{R_3}{R_2 + R_3} \times V_A$$

assuming that $V_A = V_{CC} - 1.3$.

Make sure that the swing at node B is more than 100 mV (the LVDS receiver threshold):

$$V_{ID} = \frac{R_3 \| R_T}{R_2 + (R_3 \| R_T)} \times V_{OD} > 100\ \text{mV}.$$

where V_{OD} is the differential output swing at Node A.

In a similar way, when LVDS talks to LVPECL, a step-up resistor network is necessary to boost the common-mode voltage from 1.2V to $V_{CC}-1.32V$. The only difference in architecture is that you swap V_{CC} with ground to form the step-up structure (**Figure 5**). This example does not assume any internal pull-up resistor inside the LVPECL receiver.

You can easily extend the above methodology to the interface between LVDS, LVPECL, CML, and TMDS, because TMDS and CML have similar dc characteristics. **Figures 6** and **7** are typical architectures that show how LVDS/LVPECL and CML/TMDS communicate with each other. The Thevenin voltage at Node A in **Figure 6** should be 1.2V for LVDS drivers and $V_{CC}-2V$ for LVPECL. Designers must pay attention

TABLE 2–INPUT AND OUTPUT CHARACTERISTICS OF LVPECL BUFFERS*

Transmitter with LVPECL output					Receiver with LVPECL input				
Parameter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Parameter**	**Symbol**	**Minimum**	**Typical**	**Maximum**
Output high (V)	V_{OH}	V_{CC}-1.025	V_{CC}-0.955	V_{CC}-0.88	Input high voltage	V_{IH}	Vcc-1.16		Vcc-0.88
Output low (V)	V_{OL}	V_{CC}-1.81	V_{CC}-1.705	V_{CC}-1.62	Input low voltage	V_{IL}	Vcc-1.81		Vcc-1.48
Differential output voltage (V)	V_{OD}	0.595	0.8	0.93	Differential input voltage	V_{ID}	0.3		0.93
Offset voltage (V)	V_{CM}		V_{CC}-1.32						

*V_{CC}=3.3V ± 10%.

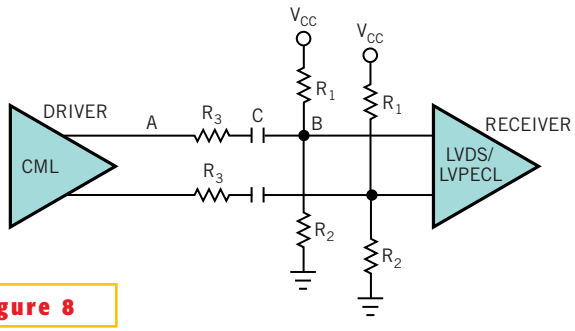


Figure 8

You use this architecture to interface CML drivers to LVDS/LVPECL receivers.

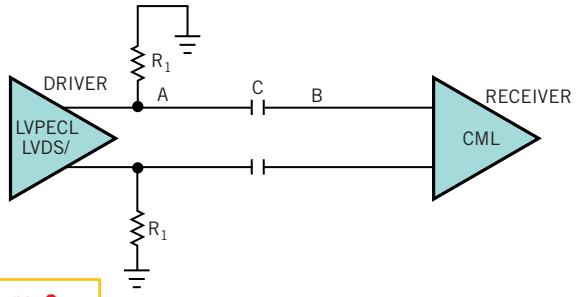


Figure 9

You can use this circuit for LVDS/LVPECL drivers interfacing with CML receivers.

to CML/TMDS receivers that typically have internal 50Ω termination resistors and consider their presence in the circuit when calculating the Thevenin equivalent resistance at Node B. You must also use parallel termination with two resistors, R_1 and R_2, in Node A, instead of one resistor tied to ground to provide the 50Ω output-impedance match for drivers and high common mode at the receiver side.

AC COUPLING

AC coupling is gaining popularity for high-speed interfaces, such as CML I/O, especially for connecting devices with different ground references. AC coupling typically needs fewer resistors than does dc coupling, but designs still need to meet several conditions:

- The input impedance of the receiver needs to match the cable characteristic impedance;
- the common-mode of the receiver needs to be at the optimal point;
- the dc bias current/voltage at the driver side must be at the proper dc operation point;
- the connection between driver and receiver requires swing compatibility; and
- the coupling capacitor must be large enough to pass the lowest data rate and meet the jitter requirement.

Figure 8 gives an example of an interconnection between CML and LVDS/LVPECL with no termination inside the receivers. Based on the general rules above, the following equations determines the chosen resistor values:

$$\frac{R_2}{R_1 + R_2} \times V_{CC} = 1.2 \text{ for LVDS and}$$
$$V_{CC} - 1.3 \text{ for LVPECL;}$$

and

$$R_1 \| R_2 = 50.$$

For the LVDS receiver, you can insert an attenuation resistor, R_3, before the ac-coupling capacitor to attenuate the CML output swing to the range that LVDS can accept ($100\text{ mV} < V_{ID} < 600\text{ mV}$). **Figure 9** is a general diagram for the ac coupling between LVDS/LVPECL and CML. For LVPECL drivers, you choose resistor R_1 so that 14 mA of dc current flows through this resistor to establish the proper dc operation point. For LVDS, you use a 50Ω resistor R_1 to set the output differential voltage swing at around 350 mV.

SIMPLIFIED OPTIONS

Many manufacturers are working on ways to eliminate the above RC networks between drivers and receivers with different types of I/O. Possibilities include a wider receiver common-mode range and programmable driver swing. For example, Fairchild has designed its new LVDS products for easy interconnection between different types of differential I/O. LVDS repeaters, such as the FIN1101/FIN1108 (8-bit version repeater); all provide a 0 to V_{CC} input common-mode range, which absolutely exceeds the TIA/EIA-644 LVDS standard requirement of 0 to 2.4V. The FIN1101 can interface directly with LVPECL/CML drivers without a resistor network. Using a PRBS (pseudorandom bit sequence) $2^{23} - 1$ data pattern with CML levels at a data rate of 622 Mbps, the differential output of Fairchild's single-bit repeater (Model FIN1101) has about 67 psec of peak-to-peak deterministic jitter, which is less than 4.2% of the eye opening. The resultant random jitter is about 1.4 psec for a 622-MHz differential CML clock input.□

AUTHOR'S BIOGRAPHY

Jeff Ju is a senior applications engineer with Fairchild Semiconductor's Switch Products Group (South Portland, ME). He earned a BSEE from Nantong Institute of Technology, Jiangsu Province, China, and an MSEE from the State University of New York—Binghamton.

TABLE 3–CML OFFERS THESE INPUT AND OUTPUT CHARACTERISTICS*

Transmitter with CML output					Receiver with CML input				
Parameter	Symbol	Minimum	Typical	Maximum	Parameter	Symbol	Minimum	Typical	Maximum
Output high (V)	V_{OH}			3.35	Differential input swing	V_{ID}	0.2		0.6
Output low (V)	V_{OL}	2.94			Receiver input signal	V_I	2.7	3.1	3.5
Differential output voltage (V)	V_{OD}	0.32	0.4	0.5					
Offset voltage (V)	V_{CM}		Vcc-0.2						

*V_{CC}=3.3V ± 5%.