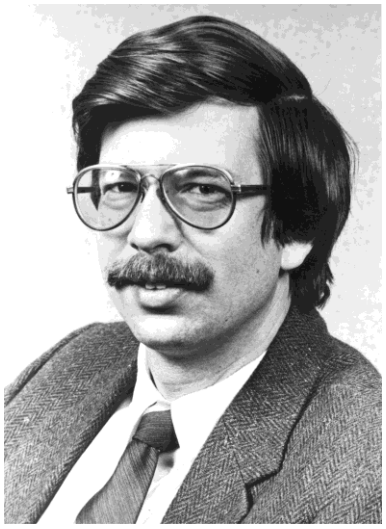
Xilinx and the Birth of the Fabless Semiconductor Industry

While working at microprocessor pioneer Zilog in the early 1980s, an engineer named Ross Freeman conceived of a new logic circuit that was reprogrammable: a single piece of silicon that could meet the needs of all of those ASIC customers. At that time, there were dozens, perhaps hundreds, of application-specific IC (ASIC) companies building custom silicon for thousands of customers. However, the design and fabrication of ASICs took months. Freeman's idea would permit the development and implementation of a custom IC in less than a day and it coincidentally hastened the birth of the fabless semiconductor industry.

Freeman earned a BS degree in physics from Michigan State University in 1969 and a master's from University of Illinois in 1971. He worked in the Peace Corps and taught math in Ghana for two years. When he returned to the United States, Freeman joined Teletype Corporation and designed a PMOS (p-type metal-oxide semiconductor) chip. Back then, PMOS calculator chips were the profitable, high-volume LSI chips to make and PMOS was the process technology of choice because PMOS logic was the easiest type of MOS logic to manufacture. Therefore, it was also the cheapest type of logic to make. Freeman then became one of the first engineers to join a new microprocessor startup named Zilog where he designed the Zilog Z80-SIO (Serial I/O) peripheral chip.

By the time he reached his early 30, Freeman was the Director of Engineering for Zilog's Components Division. He first got the idea for a new type of hardware-programmable device while working at Zilog and filed several patents. However Zilog was not interested in pursuing the concept so Freeman left Zilog to further develop his idea. The result came to be known as the FPGA.



Ross Freeman, inventor of the FPGA
(Photo courtesy of Xilinx, Inc.)

Although he had yet to develop a hardware design for this new device, the invention was impressive enough for Freeman to sway a Zilog coworker, Jim Barnett, to join him. The two of them then set out to recruit their former boss at Zilog, an experienced executive named Bernie Vonderschmitt, to become the CEO of the new FPGA start-up.

Semiconductor Business Lessons at RCA

Prior to joining Zilog, Vonderschmitt had worked for more than three decades at RCA Corp. He was hand-picked by RCA's legendary leader, David Sarnoff, to head color television development in 1953. Even though the FCC had already approved it, Sarnoff was determined to obsolete the rival CBS color TV system that was based on a mechanical, rotating color wheel before it could spread commercially.

In an agreesive project over an 18-month period, Vonderschmitt's team at RCA developed the NTSC transmission standard. Unlike the CBS version, it was backward-compatible with the existing standard for black-and-white broadcast TV signals. Although often referred to by TV engineers as "Never The Same Color," the resulting NTSC broadcast standard remained in use for half a century until finally replaced in the United States by digital HDTV and the ATSC broadcast standard in 2009.

Partly because of his success in successfully managing the NTSC color TV project, Vonderschmitt eventually became the Vice President and General Manager of RCA's Solid State Division. RCA had developed semiconductors for its own use in TVs, broadcast equipment and computers. The company waited until the late 1950s before becoming a merchant semiconductor vendor. Consequently, RCA missed the first IC manufacturing wave and did not become a major player in the early bipolar integrated circuit market like Fairchild. Instead, RCA focused on MOS integrated circuits.

In the early to middle 1960, RCA's David Sarnoff Research Center developed a way to put both P- and N-channel transistors on one chip—demonstrating feasibility in 1963 and 1964 and then developing the COSMOS (RCA's trade name for "complementary symmetry metal oxide semiconductor," better known as CMOS) line of integrated circuits in the late 1960s. Vonderschmitt became head of RCA's Solid State Division a bit later, in 1972. During that period, Seiko came to RCA's Solid State Division seeking to license a low-power semiconductor process technology to help leapfrog its wristwatch business. That's when Vonderschmitt and Seiko first connected.

Seiko Epson Corporation had its origins in Suwa Seikosha, one of several manufacturing companies in The Seiko Group. The Seiko Group evolved from K. Hattori & Company, a trading company first established in 1881 that imported and exported clocks and watches. Suwa Seikosha was the manufacturing arm of the company. It made men's watches. Seiko had foreseen the changeover from mechanical watches to all-electronic wristwatches and it wished to be on the forefront of that change. Vonderschmitt licensed RCA's CMOS process to Seiko. By 1973, the company was producing digital LCD wristwatches based on Seiko's proprietary CMOS watch chips.

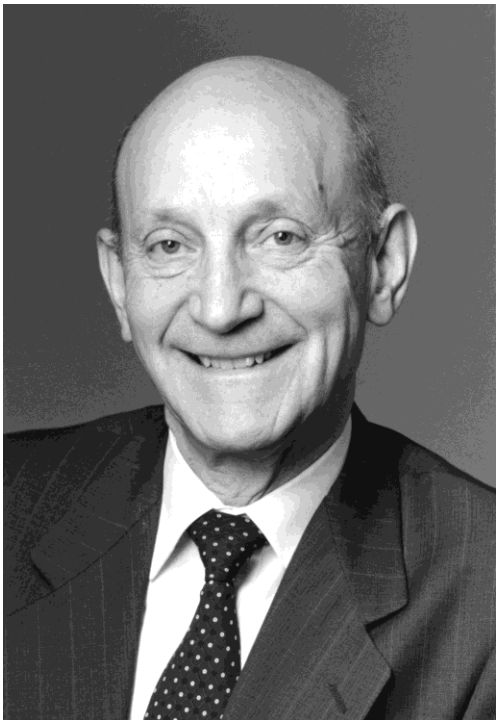
While serving as head of RCA's Solid State Division, Vonderschmitt had a clear view of semiconductor manufacturing's voracious appetite for capital; He managed the company's IC development and manufacturing businesses, overseeing three in-house semiconductor foundries. During his tenure as

division head, Vonderschmitt often had trouble obtaining capital from the parent corporation to scale new IC process technologies from the research labs to production.

Things got more difficult as RCA moved further into its conglomerate phase. David Sarnoff's son Robert Sarnoff had taken over the reins of the company in 1970 and RCA announced its termination of the general-purpose computer systems division in 1971, marking the company's initial move away from technology and the start of its conglomerate phase. Making ICs was never RCA's mainstream business. Producing televisions, broadcast equipment, TV shows, and audio recordings on vinyl LPs were RCA's main businesses. During this period, RCA acquired Hertz (rental cars), Banquet (frozen foods), Coronet (carpeting), Random House (publishing) and Gibson (greeting cards). Consequently, those businesses and RCA's M&A activities garnered the lion's share of the company's development capital leaving little for IC manufacturing growth and development.

If I Ever Start a Semiconductor Company, it will be fabless

By the end of his tenure at RCA, Vonderschmitt was convinced that captive semiconductor fabs were too expensive and too burdensome. "If I ever start a semiconductor company, it will be fabless," he vowed. "We'll find partners who can do our manufacturing for us." With these insights and his deep industry connections, Vonderschmitt had the vision and star power that Freeman and Barnett would need to secure investors for a fabless semiconductor company in 1984.



Bernie Vonderschmitt, originator of the fabless semiconductor business model
(Photo courtesy of Xilinx, Inc.)

Vonderschmitt left RCA in 1979 and decided to take time off from the industry. He used that time off to earn an MBA from Rider University. Then he joined microprocessor pioneer Zilog in Silicon Valley. However, Vonderschmitt joined Zilog after its startup days, just after it was acquired by Exxon, and he soon saw that Zilog had the same problems with getting capital for its fab and for improving its semiconductor process technology from Exxon that RCA's Solid State Division had with its parent. It was déjà vu all over again, to quote Yogi Berra, and Vonderschmitt was ready for a move when Freeman and Barnett approached him.

Vonderschmitt, Freeman, and Barnett officially founded Xilinx in February 1984.

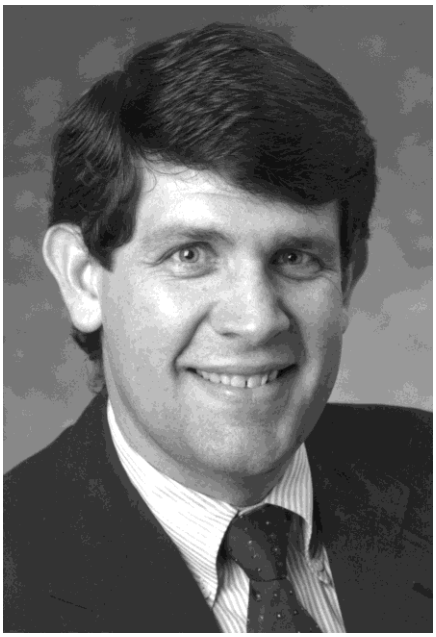
The Birth of Xilinx and the Fabless Movement

Although Freeman and Barnett convinced Vonderschmitt to found a new semiconductor company based on the FPGA's potential, he had no intention of owning fabs like RCA or Zilog. Having twice experienced the stresses and risks of owning an IC fab, Vonderschmitt planned to focus Xilinx on what Xilinx did best—designing innovative programmable devices—and to partner with others to gain access to skills and assets not within Xilinx's area of expertise—especially capital-intensive chip manufacturing.

In pursuit of his vision for a fabless semiconductor company, Vonderschmitt now leveraged his decade-long friendship with a Seiko executive named Saburo Kusama to see if Seiko would be willing to manufacture FPGAs for Xilinx. Vonderschmitt had met Kusama-san while licensing RCA CMOS technology to Seiko for its watch business.

In pitching the Xilinx proposal, Vonderschmitt convincingly argued that such a partnership would let Seiko keep its fab running at capacity to further offset its capital equipment costs and possibly even make additional profit if the Xilinx FPGAs succeeded in the market. Vonderschmitt sweetened the deal by granting Seiko exclusive reselling rights to Xilinx FPGAs in Japan. The deal was consummated largely on the basis of the friendship between Vonderschmitt and Kusama-san. The initial paper agreement was only two pages long. Xilinx's fabless business was launched.

The task of actually designing the first functional FPGA fell to a young engineer named Bill Carter, whom Freeman and Barnett recruited from Zilog in March 1984. Freeman had originally hired Carter at Zilog to work on the Z8000 microprocessor. Carter now followed Freeman to Xilinx.



Bill Carter, designer of the first FPGA
(Photo courtesy of Xilinx, Inc.)

Prior to joining Xilinx Carter had worked on NMOS microprocessors and peripherals at Zilog. He also had previous bipolar design experience but Seiko's process technology was CMOS so the Xilinx FPGA would be Carter's first CMOS design. As an added challenge, this FPGA was going to be a very large chip. Thus Carter had to figure out a way to develop a never-designed-before IC, which would be as large as a complex microprocessor, on a very tight schedule. He also had to work with an IC fab on the opposite side of the Pacific that was not accustomed to working with outside customers all while overcoming barriers of a foreign language, foreign business culture, and a foreign engineering culture.

Nothing Too Clever or Exotic

Vonderschmitt regularly advised Carter to keep the design as simple as possible and not try anything "too clever or exotic." An overly complex design could make it harder to produce a functional device and deliver it to customers on schedule. Keeping risk to a minimum was very important to Vonderschmitt. He realized that a tiny, start-up company offering a first-of-its-kind chip through a unique fabless business model could easily scare off customers.

(In fact, to downplay the risk of doing business with the new FPGA company, Vonderschmitt told would-be customers that Xilinx planned to build a fab once it hit a US $50 million run rate and would also secure a second source, as was customary—actually almost mandatory—at the time. Monolithic Memories (MMI) later signed on as Xilinx's first second source. By coincidence, MMI was subsequently acquired by AMD, run by Jerry "real men have fabs" Sanders, and so AMD became a second source for Xilinx FPGAs.)

Seiko's CMOS fab employed a 2.5µm process—a relatively mature and low-risk silicon process well suited to digital watch circuits. Consequently, Seiko manufactured chips with very conservative design rules to make chip manufacturing easier and to boost yields. The Xilinx FPGA design would not be conservative with respect to design spacing. In fact, the XC2064 FPGA would require a whopping 85,000 transistors for its 64 configurable logic blocks and 58 input/output (I/O) blocks. That was more transistors than used in the design of the Motorola 68000 32-bit microprocessor. At roughly 300 mils per side, the die size for the first Xilinx FPGA would be larger than almost anything being manufactured at that time and it would be much bigger than anything Seiko's own designers had ever attempted.

To keep the FPGA within the 300-mil spec, Carter knew he would have to pack everything as close together as possible. He pushed Seiko to thoroughly characterize its CMOS process and to provide extremely accurate minimum feature sizes.

The chip's architecture was largely based on one modular CLB (configurable logic block) and one modular I/O block. The chip's design repeated these two blocks many, many times. (Some of the edge and corner CLBs required slight variations.) The repetitive use of identical modular blocks greatly simplified the FPGA's design—enough to permit manual design and verification. Xilinx used no computer-aided design (CAD). CAD systems were too expensive for a semiconductor start-up on a shoestring budget.

Carter's design team employed extensive design reuse so that it could concentrate the bulk of its time on circuit-level design and verification. Despite Vonderschmitt's urging to keep things simple, some of the chip-design techniques that Carter used were unconventional. For example, a typical CMOS design always pairs one p-channel transistor with an n-channel device. Carter's FPGA design drew on his NMOS design experience and employed fewer p-channel and more n-channel devices, which improved performance and saved space on the chip.

The design budget did allow Carter's design team to lease SPICE simulation time on a Control Data Corporation (CDC) mainframe, accessed via a dial-up connection in those pre-Internet days. Remote SPICE simulation was extremely slow. A simple syntactic error or typo could mean many lost hours and waiting in the timeshare queue for the SPICE job to run only to have that run fail because of a silly mistake was extremely frustrating, particularly with a looming delivery deadline.

Luckily, an inexpensive PC-based SPICE simulator became available at just the right time. Carter convinced Vonderschmitt to invest in a PC, which he used to verify that the SPICE deck syntax was correct before submitting the simulation to the CDC mainframe. Although the PC ran the SPICE simulation very slowly compared to the timeshare mainframe, the elapsed time was about the same due to the additional overhead from the upload speed over a modem and the waiting time in the timeshare queue. The CDC timeshare subscription quickly went away.

The team performed all design-rule checks, including electronic CAD (ECAD) electrical rule checks to find simple errors, at the end of the design process and then manually typed the final layout's cell coordinates into a Calma digitizer, which allowed the team to finally see the complete design layout for

the first time. After further checks, the team sent the nine-layer design out to a pattern generator in preparation for mask production, which was done by Seiko. The chip taped out in late May 1985.

Ross Freeman checks a photoplot for the world's first FPGA, the XC2064
(Photo courtesy of Xilinx, Inc.)

The First FPGA Wafers Were Mostly DOA

After delivering the design to Seiko, Carter's team had to wait two months until early July, 1985 to receive the first-run silicon: a box of 25 wafers. The team applied probes, a home-brew debugger, and a curve tracer to the wafers to see if any of the chips on the wafers would power up. The first ten wafers out of the box all exhibited dead shorts between power and ground. Not a good sign.

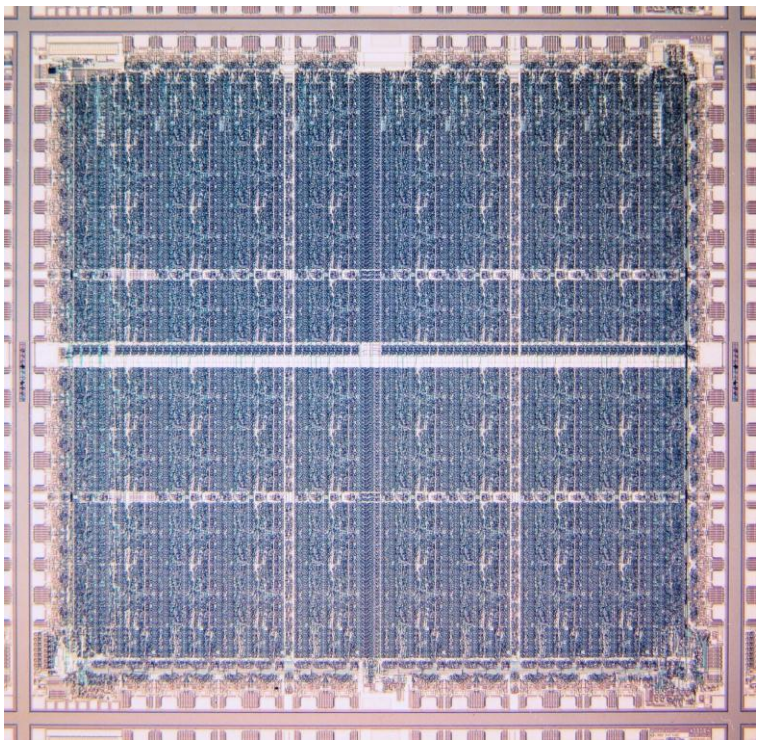
The 11th wafer showed some signs of life, and a very high current draw. The last 14 wafers also had dead shorts between power and ground. Carter's team discovered that insufficient metal etching was causing the shorts. There were aluminum whiskers causing shorts between the power and ground rails all over the first-run wafers. On the single partly dead wafer, the metal whiskers were thin enough to blow out like fuses. By applying enough supply current to a chip on the wafer, the test team managed to burn out the whiskers and open the shorts.

The now-operational chips on that one wafer were sufficiently robust to let Carter's team continue debugging the design of the FPGA. Carter was finally able to run a simple configuration bit stream into the device. After successfully programming an inverter into one of the CLBs, Carter called Freeman and Vonderschmitt while they were traveling in Japan and reported that that the "DONE line had gone high,"

and that Xilinx “had successfully created the world’s most expensive inverter.” After this initial success, the design team was able to program more and different logic circuits into the FPGA, eventually configuring all 64 CLBs on a chip.

The Birth of the FPGA

Seiko and Xilinx solved the aluminum-whisker issue that plagued the first-run batch of FPGA wafers and Xilinx received working devices in September, 1985. A press release announced the birth of the world’s first FPGA—the XC2064 (called a “Logic Cell Array” in the press release)—on November 1, 1985.



Die Photo of the XC2064, the world’s first FPGA
(Photo courtesy of Xilinx, Inc.)

In addition to providing an additional revenue stream to Seiko and helping to keep the fab full, running FPGAs with their repetitive structures through its fabs helped Seiko debug subsequent IC process technology generations, improving device yields and lowering unit costs for all of the chips Seiko manufactured. This use of FPGAs as a “process driver” help to open the door for Xilinx, giving the company access to leading-edge IC manufacturing technology at Seiko and at other semiconductor foundries. Fab vendors now want to use FPGAs as process drivers because of their ability to diagnose process problems.

Conclusion

As the value proposition for the silicon foundry business became clearer, other IDMs (independent device manufacturers) started filling their fabs and supplementing their revenue by manufacturing chips for third parties. In due course, an entirely new sub-industry consisting of dedicated, merchant semiconductor foundries emerged to service fabless semiconductor vendors and allowed even a small company of entrepreneurial designers to realize their innovations in silicon without the need to invest in a fab. The fabless revolution soon jumped into high gear and in 1994, ten years after Xilinx was founded, several fabless semiconductor companies including Xilinx formed the FSA (the Fabless Semiconductor Association, now called the GSA or Global Semiconductor Alliance) to provide a common voice to the electronics industry.

Bernie Vonderschmitt had foreseen all of these changes back in the 1970s while working for RCA. He knew from experience that fabs need more than one corporate customer to keep the fab lines filled and the lights on. He also understood that companies focused on IC design don't need to and often cannot afford to divert energy, resources, and attention to keeping their fab processes at the leading edge.

As we've ridden Moore's Law into nanometer territory through myriad tectonic IC process changes (copper interconnect, immersion lithography, high-K dielectric with metal gates, stress engineering, etc.), Vonderschmitt's fabless vision has become truer than ever. Over nearly thirty years, Xilinx has worked with more than 20 different semiconductor vendors and has partnered with ten vendors to supply its production FPGA silicon.

Vonderschmitt's vision has sustained Xilinx through three decades of FPGA leadership. The following words, written by Vonderschmitt two decades ago and published in the Xilinx Xcell newsletter, are still as accurate as the day they were written:

Making Fabless strategies Work by Bernie Vonderschmitt (1993)

Xilinx is just one of the more than 100 semiconductor companies that do not own their own fabrication facility, and use independent silicon "foundries" for fabrication services. "Fabless" companies are not a fad, their streamlined structure fits today's tumultuous, fast-moving marketplace. Being fabless allows Xilinx to concentrate on what we do best—the design and marketing of programmable logic devices.

Hewlett-Packard's announcement that it is quitting the foundry business and the recent troubles of a few fabless companies have led some industry pundits to once again question the viability of fabless semiconductor suppliers. (Hewlett-Packard is not one of Xilinx's wafer sources.) We strongly believe that the oracles predicting the demise of the fabless semiconductor are wrong. While ours is not the best business model for everyone, Xilinx and many other fabless companies will continue to succeed by establishing a win-win business relationship with our foundry partners.

The first key to a successful fabless strategy is to employ standard fabrication processes that are compatible with a variety of foundries. Xilinx FPGAs and EPLDs are based on “plain vanilla” SRAM and EPROM technologies. This allows us to benefit automatically from the industry’s latest process improvements and to establish multiple foundry sources for our products.

Multiple foundry sources ensure adequate and continuous product availability in case of disasters. Competition between foundries, as well as ongoing process and product improvements ensure that price projections are met. In contrast, fabless companies with specialized processes have fewer potential suppliers and less leverage in the “foundry market.” If a foundry agrees to a specialized process, prices inevitably will be higher due to the special attention needed to get and keep that process under control.

The relationship between a fabless semiconductor company and its foundries must be long term, based on mutual trust, and of benefit to both parties. Xilinx benefits financially by gaining access to advanced fabrication processes without huge capital investments. We can focus on innovation, providing value through the development of better products.

Our foundry partners benefit from diversifying their manufacturing capacity over different equipment markets; through Xilinx, they have gained access to a significant new market segment without incurring the expense of product and market development. Foundries minimize demand volatility through this market diversification. Assuming a long-term relationship, the foundry can improve its competitiveness compared to other manufacturers.

Xilinx’s foundries have gained a significant additional benefit—the ability to use FPGAs as process “drivers”—the technology used to drive and verify process advancements. The regularity and 100% testability of our FPGAs facilitates defect analysis and fault testing.

Our foundries have learned that by applying 10% to 20% of their capacity to FPGAs, they gain excellent rewards from process control diagnostics. The resulting improvements to their processes can be applied to their other CMOS product lines. (It should also be noted that Xilinx employs its own process experts, who work closely with our foundry partners in the development and implementation of process technology improvements.)

Thus, Xilinx can effectively drive process improvements through our working relationships with our foundry partners. But these relationships must be based on mutual benefits. In the future, as in the past, this will be a necessary ingredient for success.

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