

**Question-1:**

Give a logic level design for calculation of Y

$$Y = 4N^2,$$

where N is a 4-bit unsigned binary number.

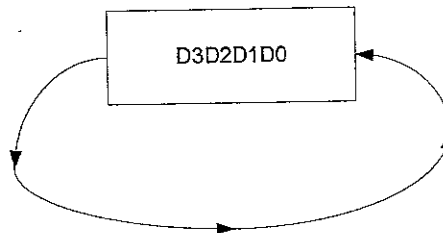
Show this implementation for N=1011. Show the input to each adder clearly. Use "0" when an input is not connected.

**Question-2:**

Design a minimum delay **14-bit Carry Select Adder**. Give area and delay performance of your adder. Show how you calculated your delay.

**Question-3:**

- a) Design a barrel shifter to do the roll(rotate left logically) instruction for 4-bits of Data  $D = D_3 D_2 D_1 D_0$ . Use 4 to 1 MUX for this circuit, for shifts of 0, 1, 2, 3. Show your input, output signals clearly and draw the selection table.



- b) Using distributed shifting(Using 2 to 1 MUXs) design barrel shifter that can shift  $D = D_3 D_2 D_1 D_0$  by up to 3 places. Shifts are to the left. Substitute 0 for data shifted.. Mark all input, output and control lines clearly.

Midterm Oct 13, 2011  
 Question 1

COEN 6501

$n_3 \ n_2 \ n_1 \ n_0$

$n_3 \ n_2 \ n_1 \ n_0$

$n_3 n_0 \ n_2 n_0 \ n_1 n_0 \ n_0 n_0$

$n_3 n_1 \ n_2 n_1 \ n_1 n_1 \ n_0 n_1$

$n_3 n_2 \ n_2 n_2 \ n_1 n_2 \ n_0 n_2$

$n_3 n_3 \ n_2 n_3 \ n_1 n_3 \ n_0 n_3$

$n_3 n_2 \ n_3 n_1 \ n_3 n_0 \ n_2 n_0 \ n_1 n_0 \ 0 \ n_0$

$n_3$

$n_2 n_2$

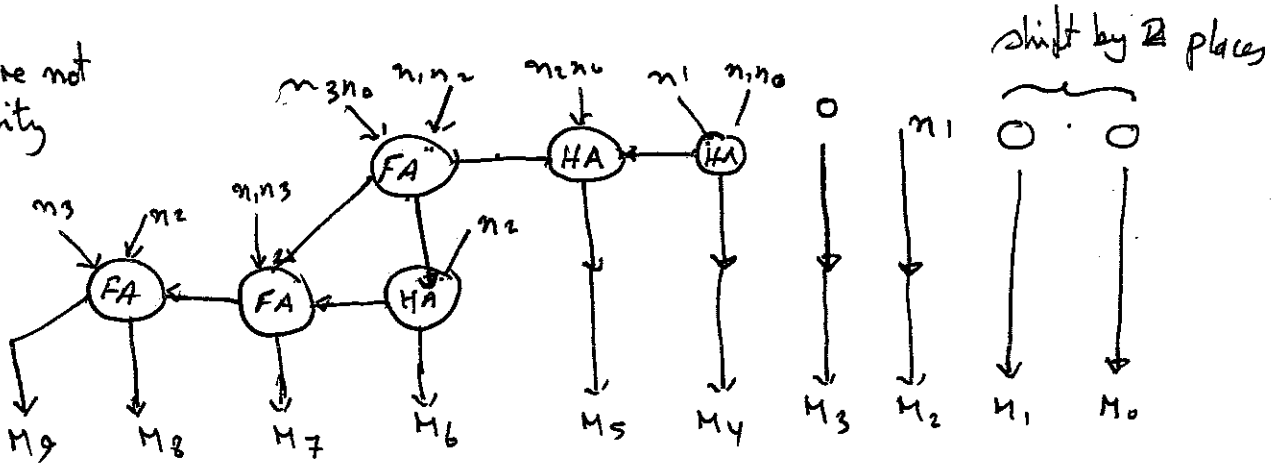
$n_1$

$n_2$

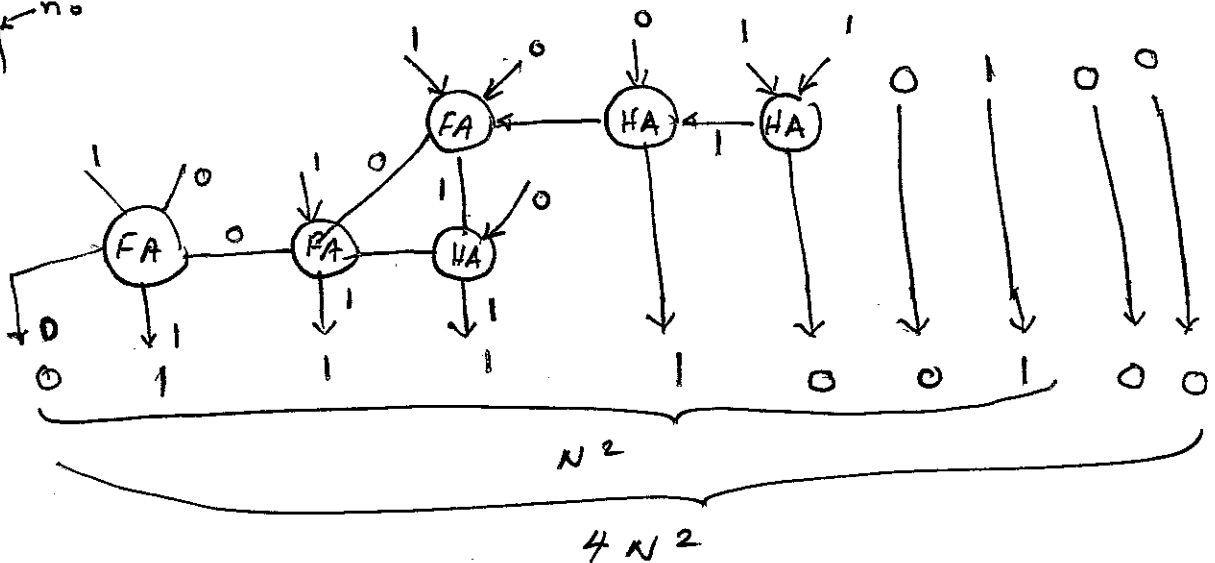


$PP_{ij}$

AND gates are not shown for clarity



$n_3 \ n_2 \ n_1 \ n_0$   
 $N = 1011$



Total area required  $\rightarrow 3FA + 3HA$

Delay of the circuit  $\rightarrow 3\tau_{FA} + 3\tau_{HA}$

Q 2

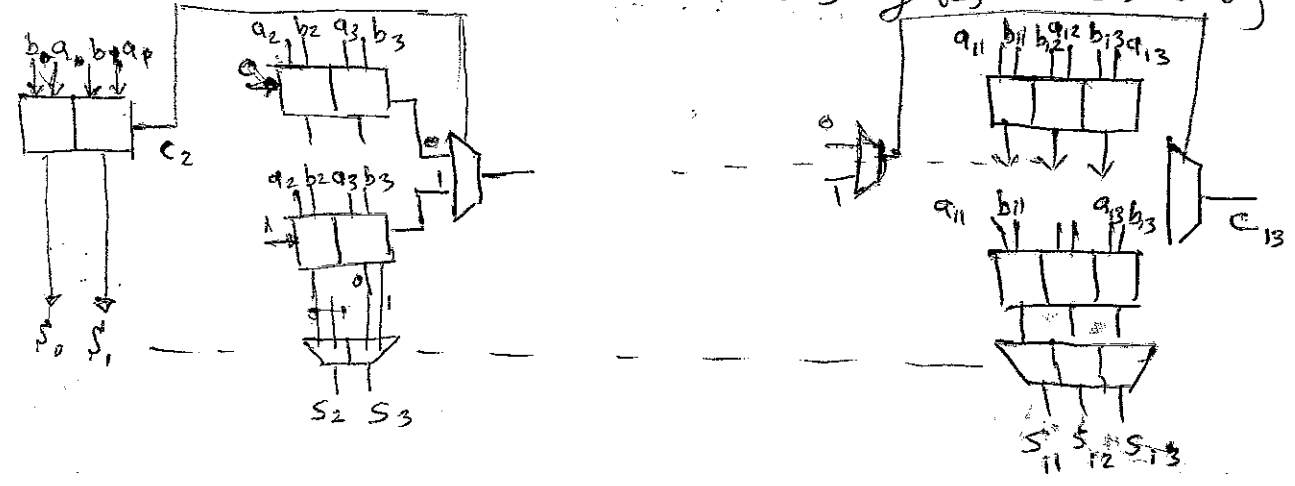
There is many way that this CSA can be divided :

- 2 2 2 2 2 2 2  $\xrightarrow{\text{delay}} 2 + 6/2 = 5$
- 3 3 2 2 2 2 2  $\xrightarrow{\text{delay}} 3 + 6/2 = 6$
- 3 3 3 3 2  $\xrightarrow{\text{delay}} 3 + 4/2 = 5$
- \* 2 2 2 2 3 3  $\xrightarrow{\text{delay}} 2 + 5/2 = 4 1/2$
- 2 3 3 3 3  $\xrightarrow{\text{delay}} 3 + 4/2 = 5$
- \* 2 2 3 3 4  $\xrightarrow{\text{delay}} 4 + 1/2 = 4 1/2$
- 4 4 4 2  $\xrightarrow{\text{delay}} 4 + 3/2 = 5 1/2$
- 5 5 4  $\xrightarrow{\text{delay}} 5 + 2/2 = 6$
- 3 3 4 4  $\xrightarrow{\text{delay}} 4 + 2/2 = 5$
- etc

Assuming  $C_{MUX} = 1/2 C_{FA}$

\*  $[2 + [3 * 4]_{i4}] + [3 * 2 * 2]_{i2}^{FA} + [3 * 2 + 2 *]_{MUX}$

According to the above search 2 2 2 2 3 3 gives the best delay



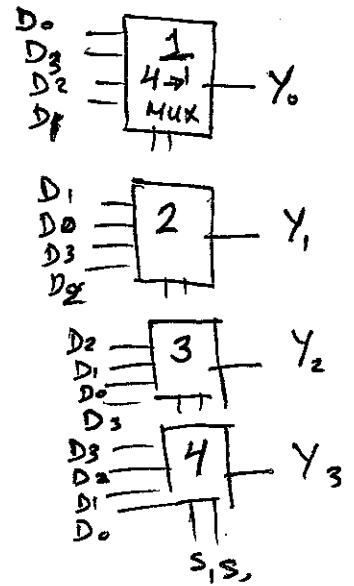
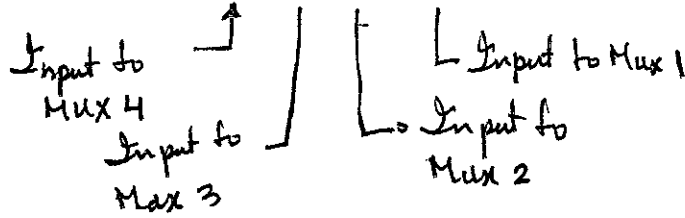
Total Delay  $\rightarrow 4 1/2 C_{FA}$

Total Area  $\rightarrow 26 FA + 12 MUX \rightarrow 1$

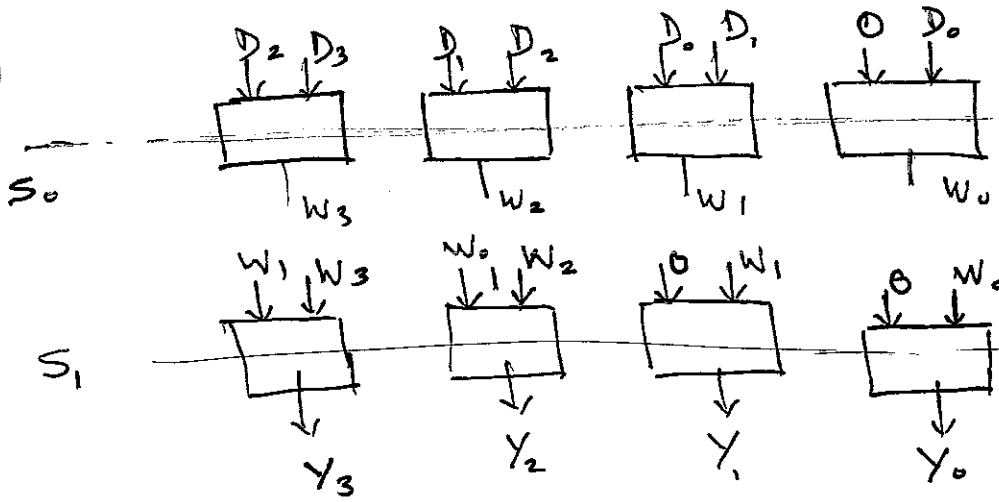
Q<sub>1</sub>

d)

S <sub>1</sub> , S <sub>0</sub>	Y <sub>3</sub> Y <sub>2</sub> Y <sub>1</sub> Y <sub>0</sub>
0 0	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>
0 1	D <sub>2</sub> D <sub>1</sub> D <sub>0</sub> D <sub>3</sub>
1 0	D <sub>1</sub> D <sub>0</sub> D <sub>3</sub> D <sub>2</sub>
1 1	D <sub>0</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub>



b)



S <sub>1</sub>	S <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	0
1	0	D <sub>1</sub>	D <sub>0</sub>	0	0
1	1	D <sub>0</sub>	0	0	0