EE 3714 Test #3 Solution - Fall 2001 – Reese

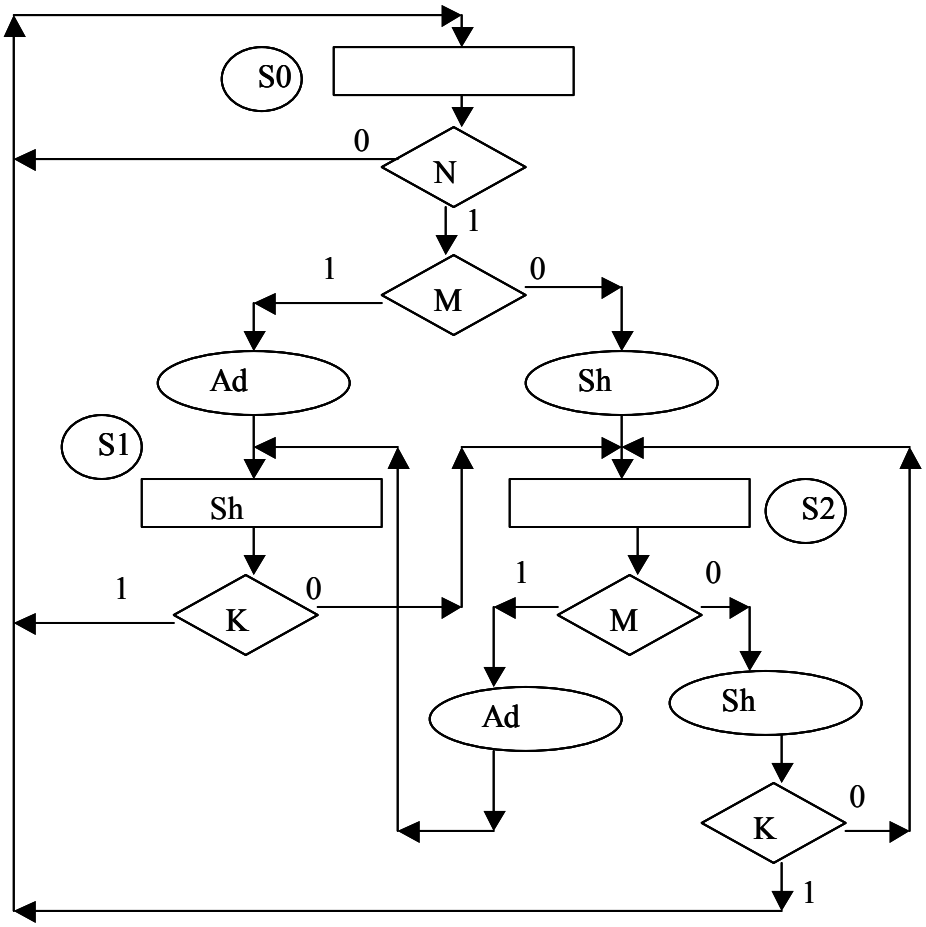
Work all problems.

1. (15 pts) For the ASM chart shown below, the state encoding is one-hot using S0=001, S1=010, S2=100.

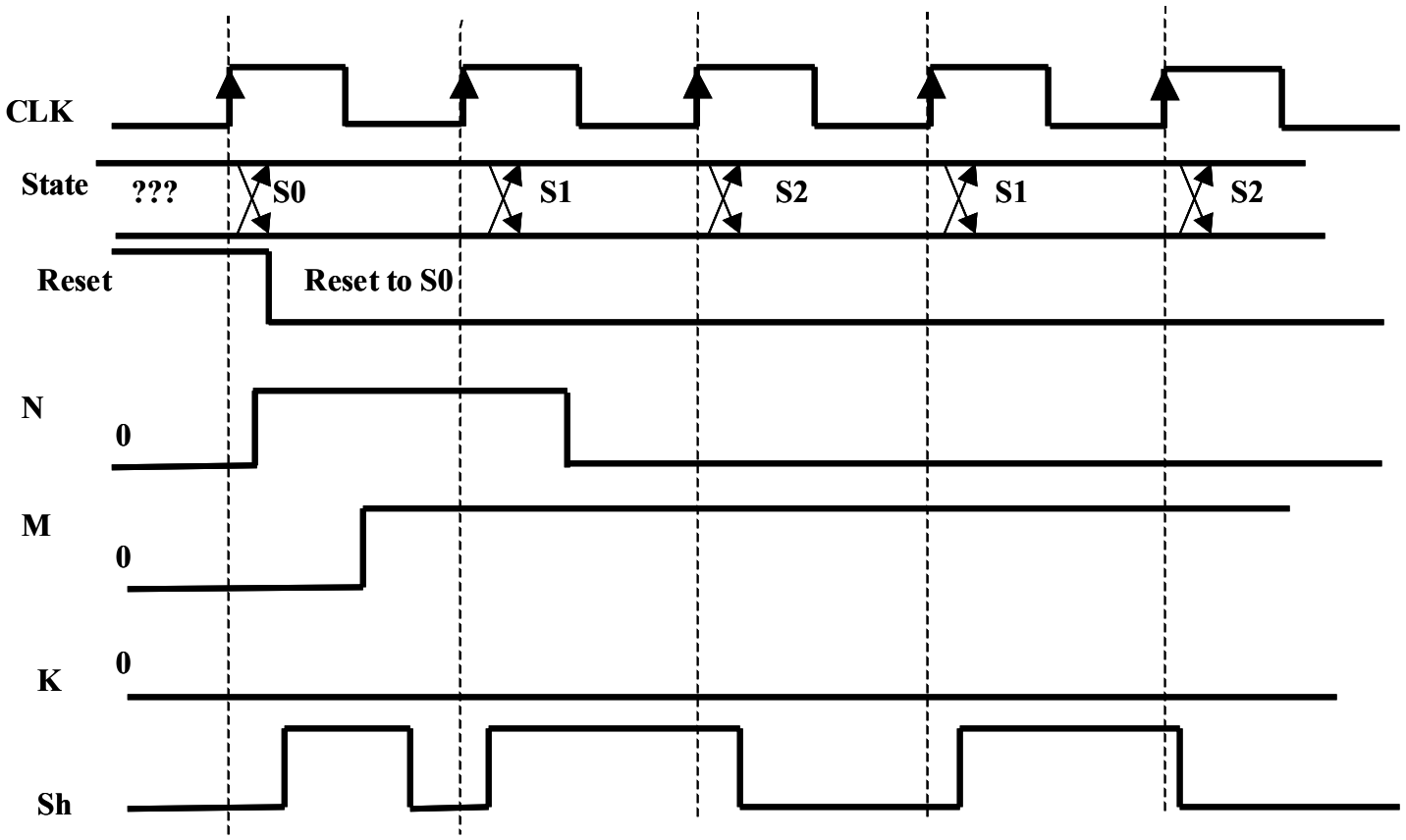
a. Write the boolean equation for the D1 input (D input for state S1 D-Flip-flop)

D1 = Q0 N M + Q2 M

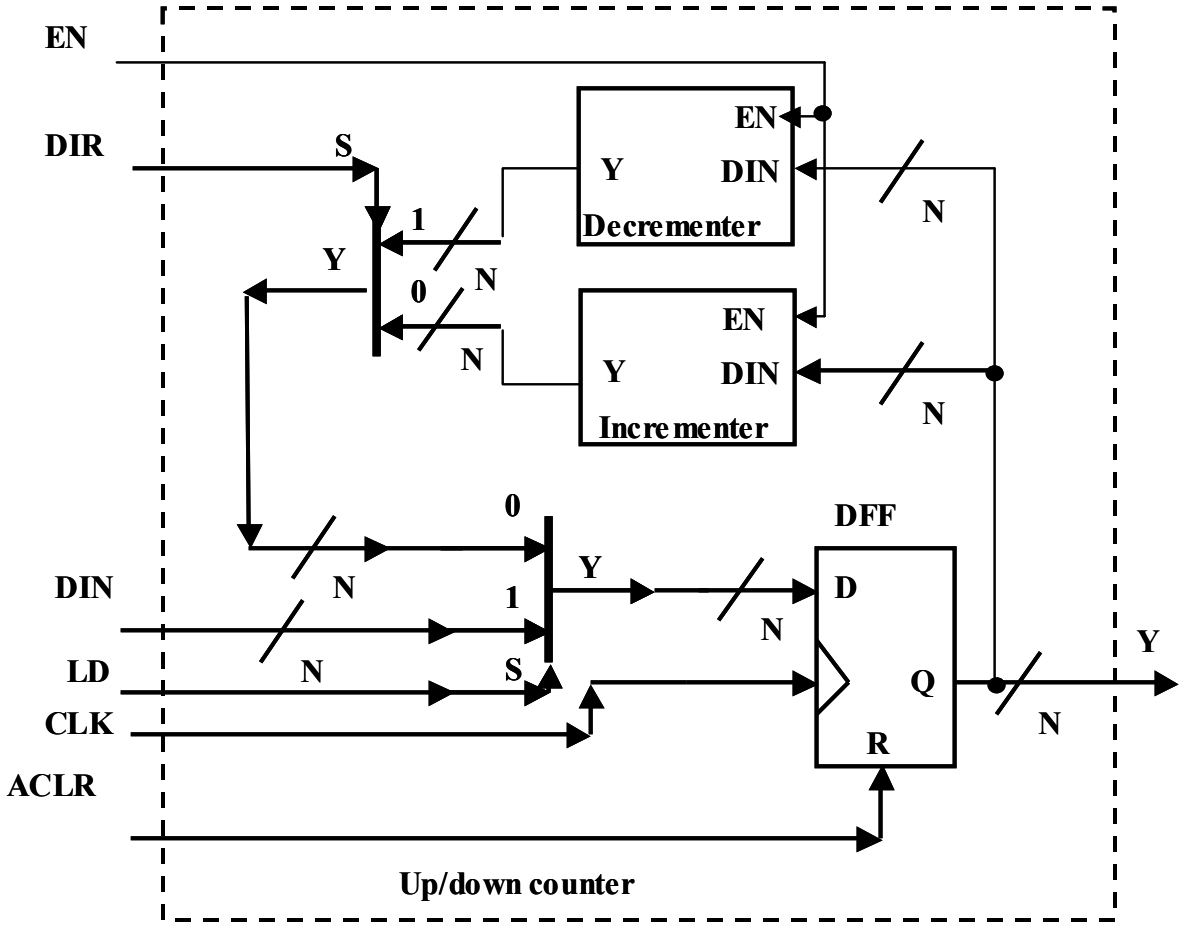
b. Write the boolean equation for the "Sh" output. *Sh = Q0 N M' + Q1 + Q2 M'*



2. (15 pts) For the ASM chart in Figure #1, complete the timing diagram below for the State and "Sh" waveforms. Assume that rising edge triggered DFFs are used for the FSM implementation. Make sure you complete the waveforms for State, Ad through the last clock cycle.

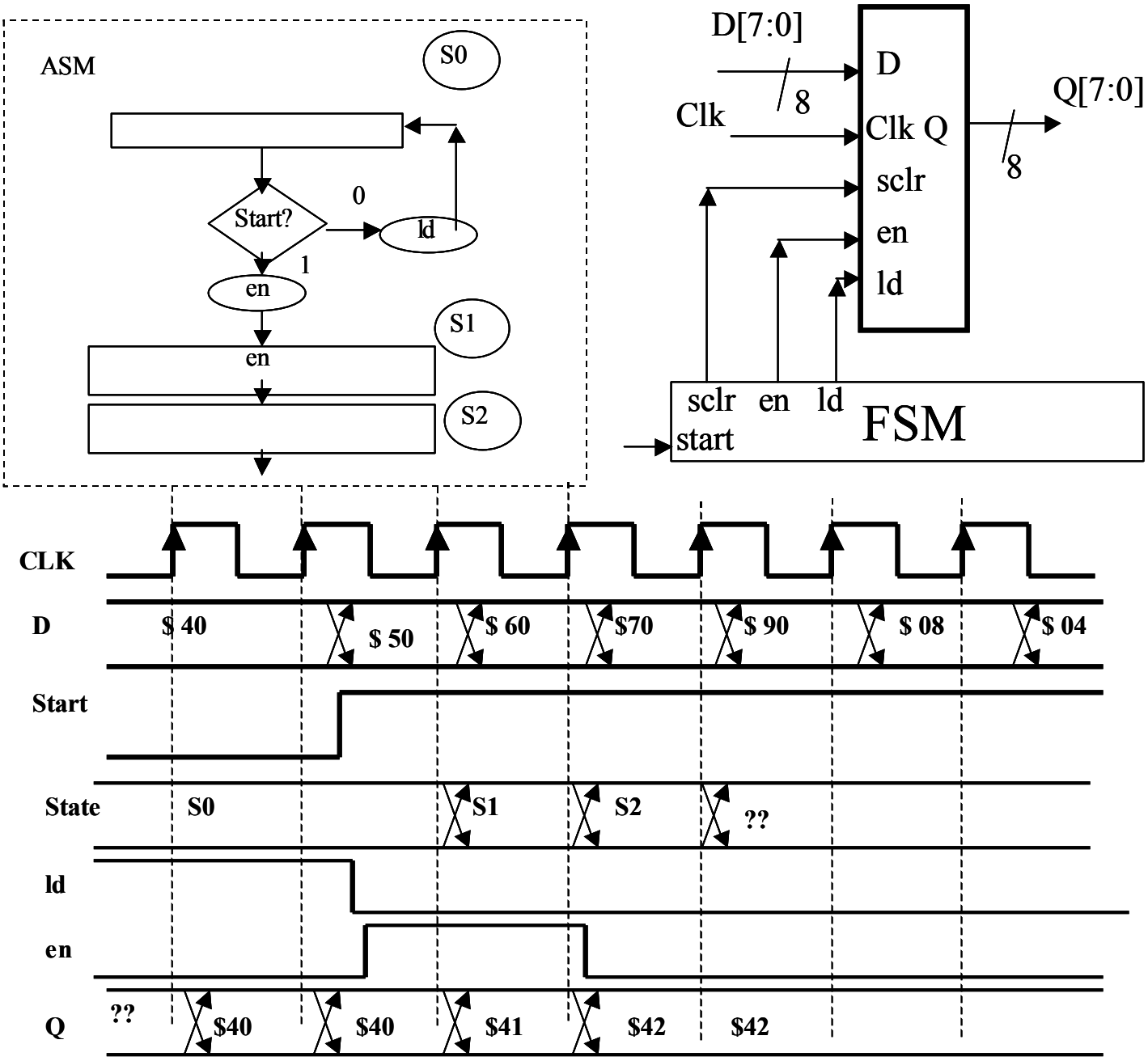


3. (20 pts) For the counter shown below, give the control input values needed for the operations listed in the table. For input values, use the symbols X (don't care), 'H' (high), 'L' (low) and ↑ (rising edge).

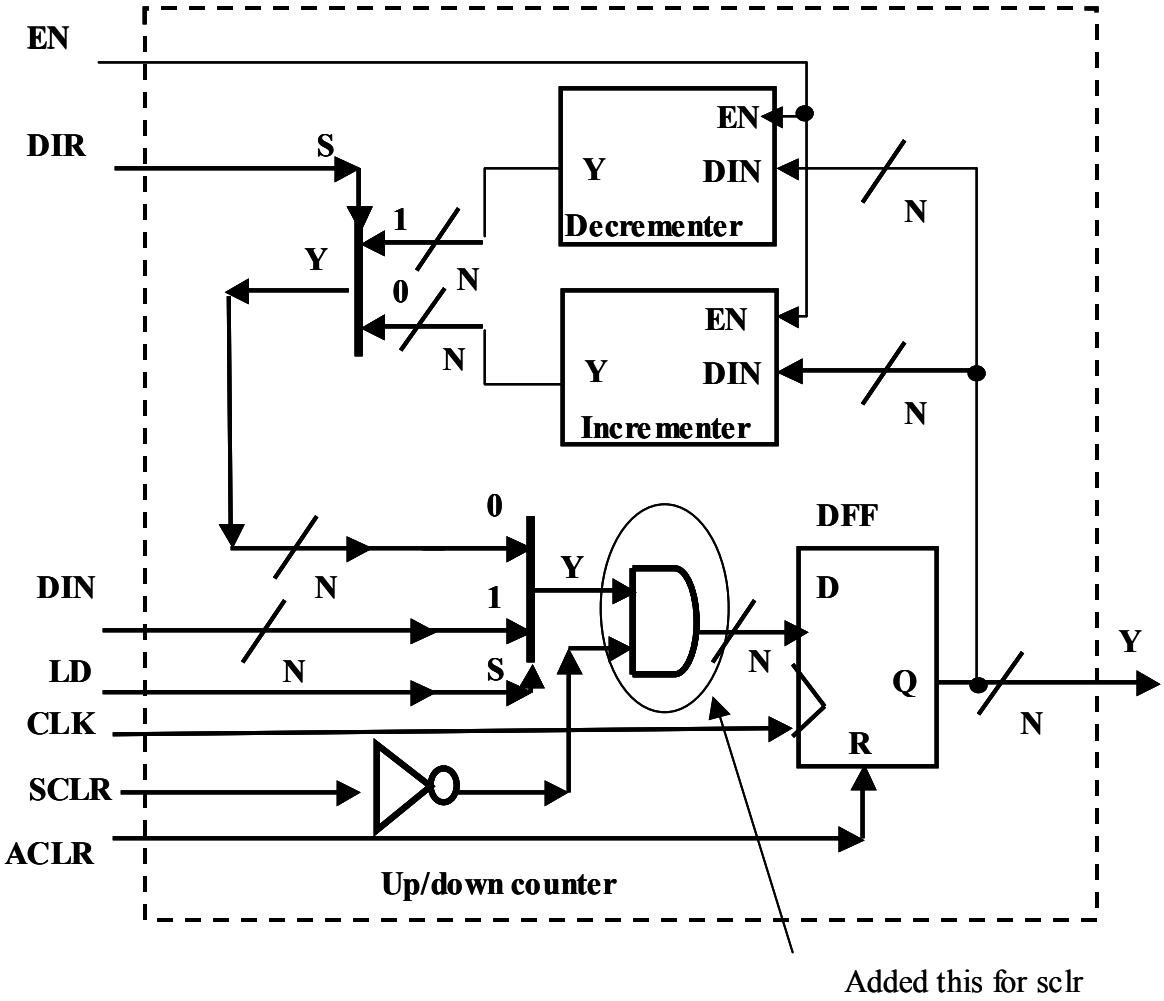


Operation	CLK	ACLR	LD	DIR	EN
HOLD (Y = Yold)	X or ↑	L	L	X	L
LOAD (Y = Din)	↑	L	H	X	X
Increment (Y=Yold+1)	↑	L	L	L	H
Decrement (Y=Yold-1)	↑	L	L	H	H
Asynchronous Clear	X	H	X	X	X

4. (20 pts) The ASM chart below specifies the behavior for the FSM that is controlling the counter that is shown. On the timing diagram, fill out the waveforms for the State, ld, en, and Q values given the Start and D values shown. Draw the waveforms through state S2 of the ASM. Assume the counter and FSM are rising edge trigerred.



5. (10 pts) For the counter below, add a SYNCHRONOUS CLEAR capability that takes precedence over the other control lines.



6. (10 pts) a. For the ASM chart in problem #1, list the states in which output *Sh* is a 'conditional' output.

States S0, S2 (Sh in oval circles)

b. For the ASM chart in problem #1, list the states in which output *Sh* is an 'unconditional' output.

State S1

7. (10 pts) Show the gating that will implement the high level VHDL statement below (CNT is a 3 bit bus):

Y <= '1' when (CNT = "011" or CNT = "101") else '0';

Y = CNT2' CNT1 CNT0 + CNT2 CNT1' CNT0