EE 3714 Test #1 Solutions - Fall 1999 – Reese

1. (6 pts) What is the minum number of bits that I need if I want to encode 24 distinct items? *5 bits can encode 32 items, 4 bits can encode 16 items, so correct answer is 5 bits.*

2. (6 pts) What range of signed integers can I represent using 6 bits and 2's complement representation? *–32 to + 31.*

3. (6 pts) The following 8-bit hex number $D3 represents a signed integer in 2's complement format. What is its decimal value? *The MSB is a '1', so number will be negative. $D3 = 11010011. Take 2's complement for magnitude, get 00101101 = $2D = 2*16 + 13 = 45. Answer is – 45.*

4. (6pts) The following 8-bit hex number $21 represents a signed integer in signed magnitude format. What is its decimal value? *MSB is 0, so number is positive. To get magnitude, just covert to decimal. $21 = 2*16 + 1 = 33. Answer is +33.*

5. (6 pts) Convert the following number decimal -15 (negative fifteen) to an 8-bit representation using one's complement format. *15 converted to 8 bits is = $0F = % 00001111. Takes ones complement to get negative representation, so answer is % 11110000 = $F0.*

6. (6 pts) Write a sum of two 8-bit hex numbers in 2's complement format that will produce a signed overflow. *$70 + $10 = $80. Positive + Positive = Negative.*

7. (6 pts) Write a sum of two 8-bit hex numbers representing unsigned numbers that will produce a unsigned overflow. *$FF + $01 = $00. 255 + 1 = 256. The value 256 is outside the range 0 to 255.*

8. (6 pts) Convert the following expression to a POS form: PQ + XY
Use distributive law $PQ + XY = (PQ + X)(PQ + Y) = (P+X)(Q+X)(P+Y)(Q+Y)$

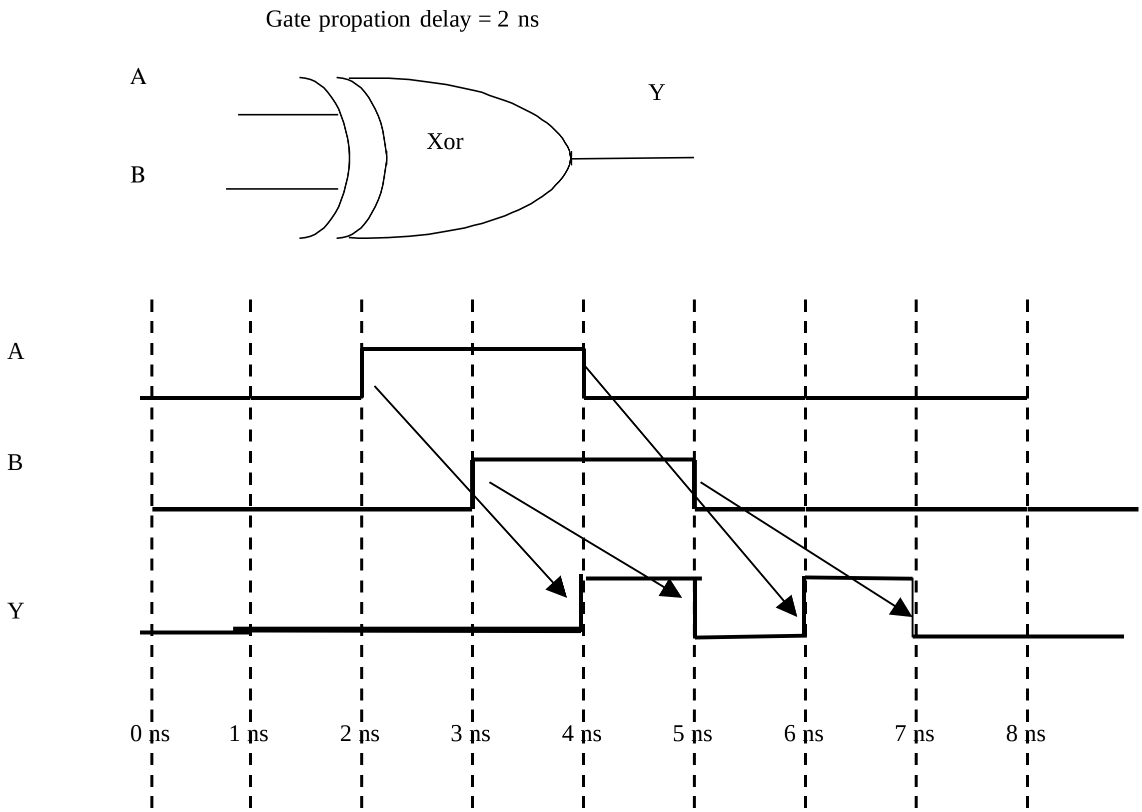
9. (6 pts) Write the truth table for the following function: F (A,B,C) = (A xor B) and C

A B C	A xor B	(A xor B) and C
0 0 0	0	0
0 0 1	0	0
0 1 0	1	0
0 1 1	1	1
1 0 0	1	0
1 0 1	1	1
1 1 0	0	0
1 1 1	0	0

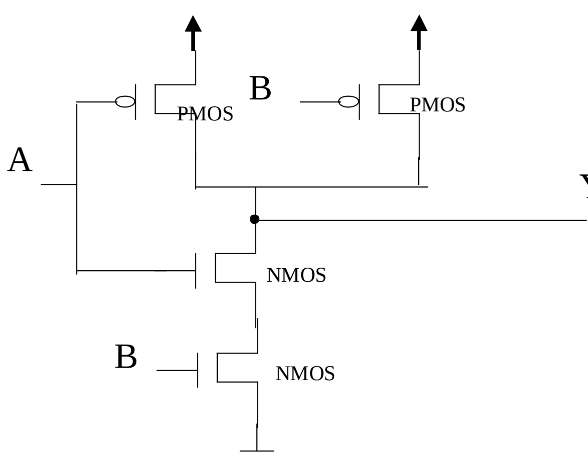
10. (6 pts) Simplify the following equation to as few as terms as possible.
$(A + (BC)')\ (A + BC)$

Use the property that $(A + X')(A + X) = A$. *Let* $X = BC$. *Then answer is* A.

11. (6 pts) Complete the timing diagram for the Y output.



12. (6 pts) Draw the CMOS transistor diagram for a 2 input NAND gate.



13. (6 pts) Convert the following to a POS form (Hint: use DeMorgan's Law):
    $(X + Y'Z)' = (X')(Y'Z)' = X'(Y + Z')$

14. (6 pts) In the circuit labeled FIGURE 1, what is the MAXIMUM path delay if the propagation delay of the inverters is 1 ns, the AND gate propagation delay is 2 ns, and the OR gate propagation delay is 5 ns?

See Figure 2.15 (c) in the textbook.
The maximum path delay is through the lower AND gate to the output:
AND (2ns) + OR (5 ns) + OR (5 ns) + AND (2) = 14 ns

The paths through the upper AND gate is:
AND (2ns) + OR (5 ns) + NOT (1 ns) + AND (2ns) + AND (2 ns) = 12 ns

15. (10 pts) For the statements below, fill in the blank using words from the list below:
    WAFER, DIE, PACKAGE, VIH, VIL, VOH, VOL, TTL, NMOS, PMOS, CMOS, NAND-NAND, NOR-NOR

a. ___*PACKAGE*____ Used to provide external connections of the inputs, outputs of the chip, placed on a printed circuit board.

b. _____*CMOS*________ The process technology in which NMOS, PMOS transistors are created; the dominant process techology for making designs with large numbers of logic gates.

c. ___*VOH*________ The minimum OUTPUT VOLTAGE that is considered to be a HIGH voltage.

d. ____*NOR-NOR*________ This two level form can implement POS equations assuming dual rail inputs.

e. _____*WAFER*_______ Processed in batches of 25 on the fabrication line; is circular and is usually either 6" or 8" in diameter, made of silcon.

16. (6 pts) Give me an example of a boolean equation that can be simplified using the consensus theorem. Give me the equation BEFORE and AFTER simplification via the consensus theorem.

    $X'Y + XZ + YZ = X'Y + XZ$