

DFFs are most common

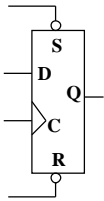
- Most programmable logic families only have DFFs
- DFF is fastest, simplest (fewest transistors) of FFs
- Other FF types (T, JK) can be built from DFFs
- We will use DFFs almost exclusively in this class
 - Will always use edge-triggered state elements (FFs), not level sensitive elements (latches).

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1

Synchronous vs Asynchronous Inputs

Synchronous input: Output will change after active clock edge
Asynchronous input: Output changes independent of clock



Flip-Flops often have async set, reset control.

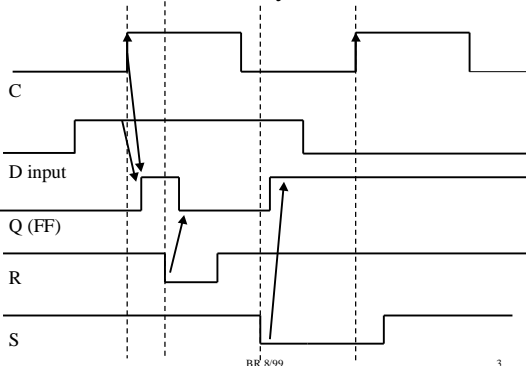
D input is synchronous with respect to Clk

S, R are asynchronous. Q output affected by S, R independent of C. Async inputs are dominant over Clk. S,R inputs often called Pre (preset) and Clr (clear) inputs.

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2

DFF with async control



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3

Flip-Flop, Latch Timing

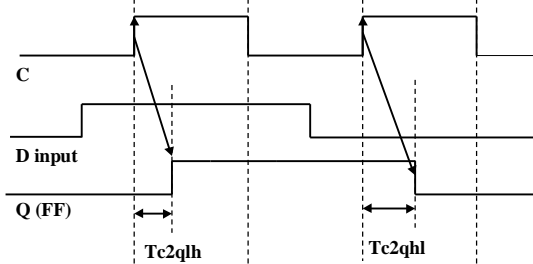
- **Propagation Delay**

- C2Q: Q will change some propagation delay after change in C. Value of Q is based on D input for DFF.
- S2Q, R2Q: Q will change some propagation delay after change on S input, R input
- Note that there is NO propagation delay D2Q for DFF!
- D is a **Synchronous** INPUT, no prop delay value for synchronous inputs

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4

Clock to Q Propagation Delay

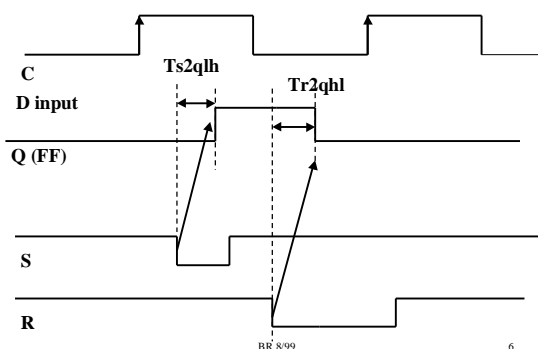


There is NO delay from D to Q!!! The clock input is what triggers the change, not the D input!!!

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5

S, R to Q Propagation Delay



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6

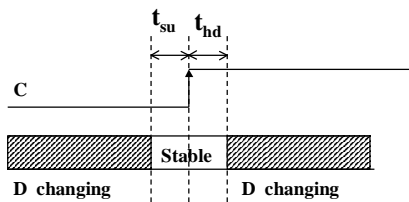
Setup, Hold Times

- Synchronous inputs (e.g. D) have Setup, Hold time specification with respect to the CLOCK input
- Setup Time: the amount of time the synchronous input (D) must be *stable before* the active edge of clock
- Hold Time: the amount of time the synchronous input (D) must be *stable after* the active edge of clock.

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7

Setup, Hold Time



If changes on D input violate either setup or hold time, then correct FF operation is **not guaranteed**.
Setup/Hold measured around active clock edge.

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8
