The new ESA 32bit processor chipset is a fundamental building block for the next generation of space systems. SPACEBEL Informatique developed a series of tools that provide valuable help in developing and testing characterised and dependable hardware and software systems.

ERC32 Tools

Considering a Design with the ERC32 Chipset?

Get Started Now!

Getting Started

When you are considering using the ERC32 chipset in a design, don't wait any longer. All tools are available to assist you with the specification, design and development of what could become the best system you ever created.

Besides the traditional software development tools, there is a series of tools that can help you from day one till the maintenance phase.

This is a unique opportunity. During all phases of the development, starting with the specification:

- use a Worst Case Execution Time Estimator to provide worst case execution paths,
- use the **Schedulability Analyser** to assess feasibility,
- use the **Target Simulator** to measure critical timing parameters,
- use the **Scheduler Simulator** to visualise and further refine the model.

When the full dynamics and size of the system are understood, then define the final hardware parameters such as CPU clock frequency, memory size and speed, ... More than 90 % of the software can be validated without hardware.

The tools provide validation capability for some of the software that cannot be validated on the hardware, such as exceptions, interrupt nesting, collisions and temporal correctness.

Verify hardware interfaces and performance before committing to silicon and hardware.

SPACEBEL Informatique's Schedulability Analyser, Scheduler Simulator and Target Simulator are new productivity tools that will assist you with your ERC32 based system development challenge.

Better tools means better control of quality, performance, project and cost.

Target Simulator

SPARC ERC32

The Target Simulator simulates a complete ERC32 based computer. The tool is exceptional in several aspects:

- Besides its simulation of the Integer Unit and its FPU and memory subsystem, it simulates more asynchronous events, such as timers, interrupts, DMA, UART, register level and data level I/O activity.
- It simulates precisely several ASIC's that have been developed for the space industry: the MEC (Memory Controller) and the ATAC (Ada Tasking Accelerator).
- The Target Simulator provides a clock cycle simulation timing accuracy while providing visibility on the internal hardware that exceeds the facilities of an In-Circuit Emulator. It allows to single step interrupt routines and inject interrupts and errors.
- It is based around the very productive Tcl command line interpreter, which is further used for the additional interfaces: the I/O Simulator, the OS Emulator, the environment simulator and the scoreboard windows.
- The user defined scoreboard window provides the information that is really needed at each break.
- The tool has many flexible interfaces that provides integration facilities through UNIX pipes, which makes it possible to integrate the tool in a more global system-wide simulator and test environment.
- The Target Simulator provides seamless integration with the Thomson Software Products' ADA cross development tools. Moreover, it works perfectly in standalone mode too, using other compiler outputs. It supports all industry standard file formats.
- Ultra-fast loading and fast simulation, approaching 1 % of the real-time, enables improved characterisation and validation in all phases of the development cycle, while significantly reducing the need for simulation, prototype and flight hardware.
- The complete hardware context can be saved and reloaded, thereby allowing to repeat rapidly critical tests within long sequences, as required for deep space validation.

The Target Simulator has been designed as a productivity tool that can be adapted for a specific board and to a specific user, and to be integrated in development and validation benches.

ERC32 Tools

You can start development of ERC32 based systems right now. With Spacebel Informatique's Target Simulator, Scheduling Simulator and Schedulability Analyser, you can maintain your grip on a complex system from the specification till the maintenance phase.

ERC32 Schedulability Analyser

The *Schedulability Analyser* provides a means to analytically verify, before execution time, that the timing constraints that apply to a real-time application are attainable. It also allows the user to assess the sensitivity of the system to changes in timing characteristics (task execution time, period, deadline) providing a means of tuning and increasing system efficiency and performance.

The Schedulability Analyser is used in an iterative way throughout the software life cycle of hard real-time applications. During the requirement and design phases the scheduling analysis is based on initial estimates of the proposed code execution time and on an initial model of thread interactions. These initial inputs are refined as the design process is carried out. Once the code is produced, a more accurate schedulability analysis can be performed.

As a result of the above activities, the design can either be reviewed or the Ada source code optimised. The highlight of areas with tight schedules and the analysis of missed deadlines are two indicators of the components to be redesigned or optimised. Sensitivity analysis allows the system designer to determine if optimisation is required and where to focus the efforts to obtain a schedulable system, therefore avoiding unnecessary or arbitrary optimisation.

The schedulability analysis is based on techniques determined from fixed priority scheduling theory. It uses an application model driven by the information required to apply these techniques.

The Schedulability Analyser also uses a computational model of the Ada runtime system to precisely quantify the system operations overheads.

The following fixed priority scheduling theories are supported by the tool:

- Fixed Priority Scheduling with deadline prior to period, commonly referred to as the Deadline Monotonic Scheduling theory.
- Fixed Priority Scheduling with Arbitrary deadlines or Arbitrary Deadline Scheduling.

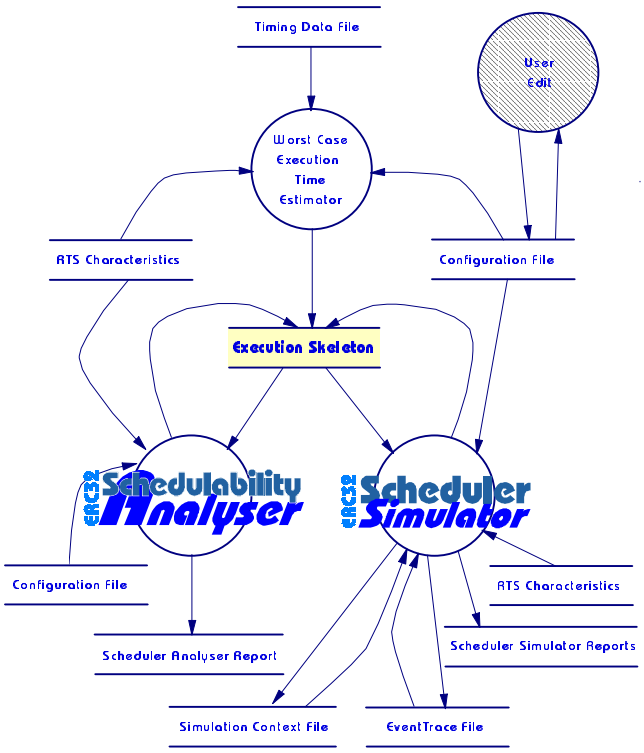
Under both theories, threads only interact through Protected Objects. Protected objects ensure critical region access through a blocking protocol. Two blocking protocols are supported by the tool:

- Inhibit Interrupt,
- Immediate Priority Ceiling Inheritance.

ERC32 Scheduler Simulator

The Scheduler Simulator provides a real-time system designer with the means to visualise the execution of a task set and scheduling characteristics. The visualisation provides the ability to investigate the circumstances under which deadlines are missed, the tightness of schedules and the CPU utilisation. The Scheduler Simulator complements the Schedulability Analyser's formal approach by showing how the designed system responds under different release patterns for interrupts and when relaxing the critical instant assumption.

The Scheduler Simulator provides the user with detailed reports and summaries of the progression of a task set and the supporting ADA run-time. The characteristics are presented through the display of *scheduling events* that occur during the modelled application's execution lifetime. The scheduling events are displayed either in graphical form or textual. The display is not dynamically generated whilst the simulation is in progress but generated after the simulation has ended.



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SPACEBEL INFORMATIQUE s.a.

Spacebel Informatique is an engineering company that specialises in dependable, real-time, parallel, reusable object oriented systems for the various space segments