SOPC WORLD 2002

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Quartus II 2.1
(LogicLock/Timing Closure)

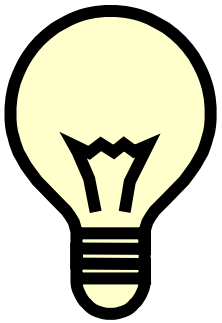
ALTERA.

Agenda

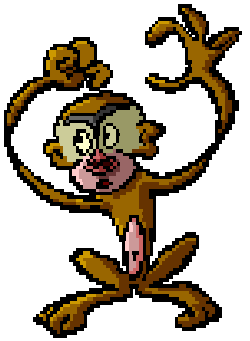
- Timing Closure Flow
- Netlist Optimization
- Design Analysis
- Timing Closure Assignments
- Summary

What is Timing Closure?

A Concept!



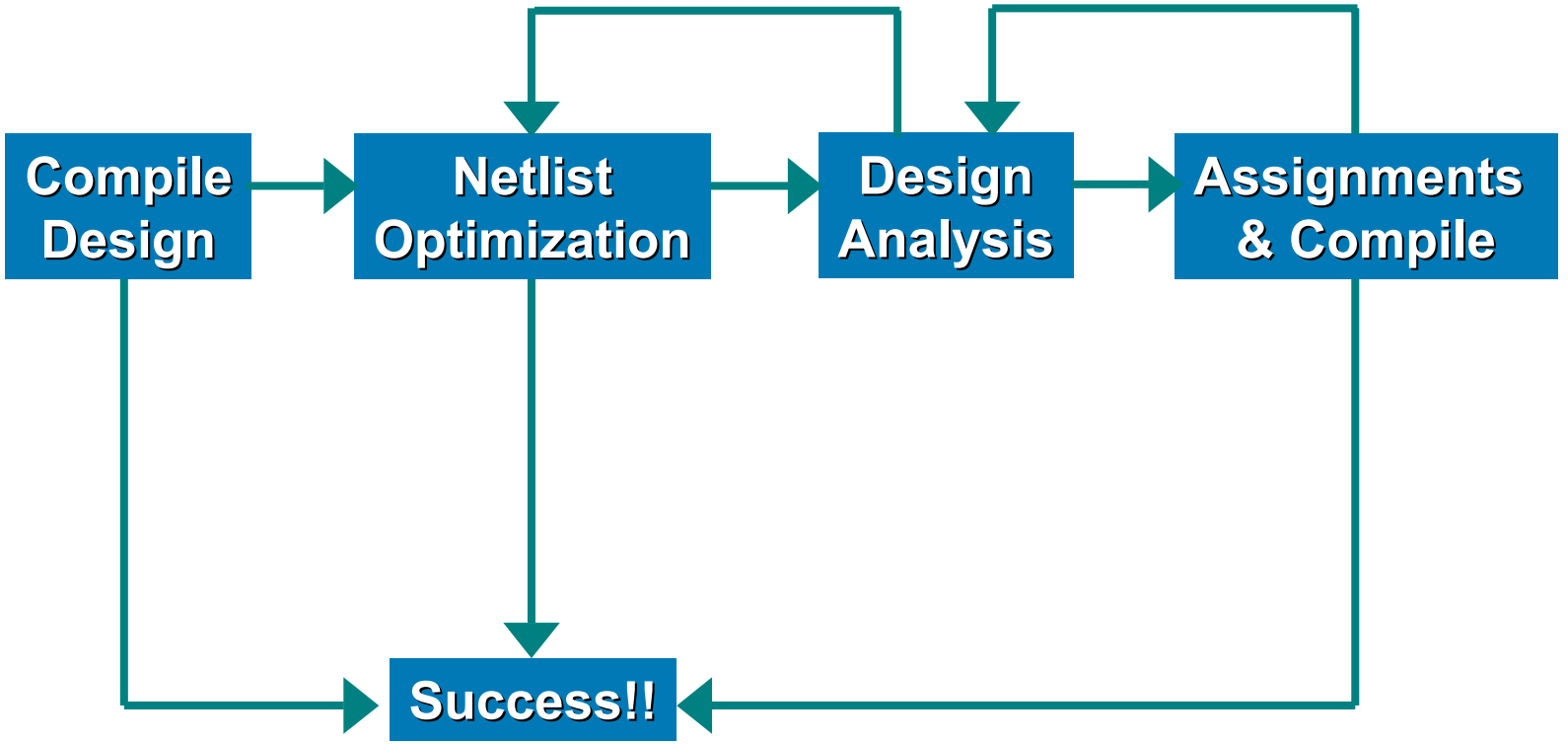
Way to Achieve Timing Requirements on a Design!



What Does Quartus II Version 2.1 Offer?

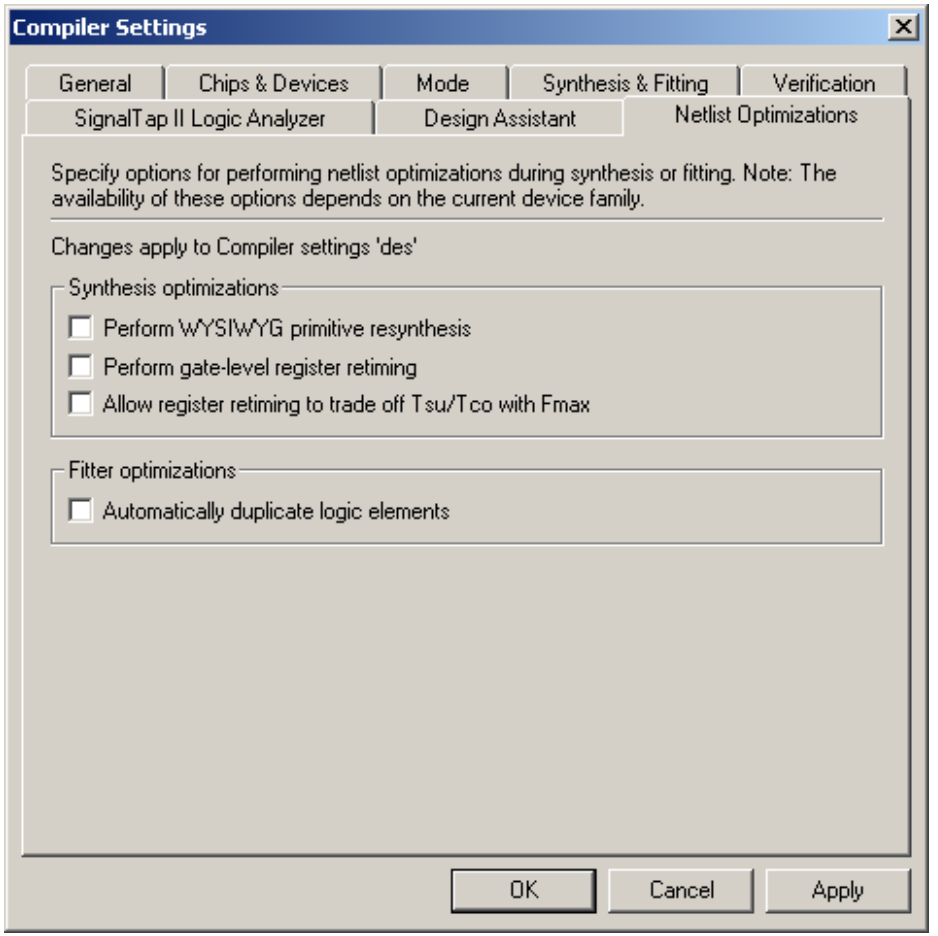
- New Tools to Help Achieve Timing Closure
  - Timing Closure Floorplan
  - Netlist Optimization Options
  - Path-Based Assignments

Timing Closure Flow



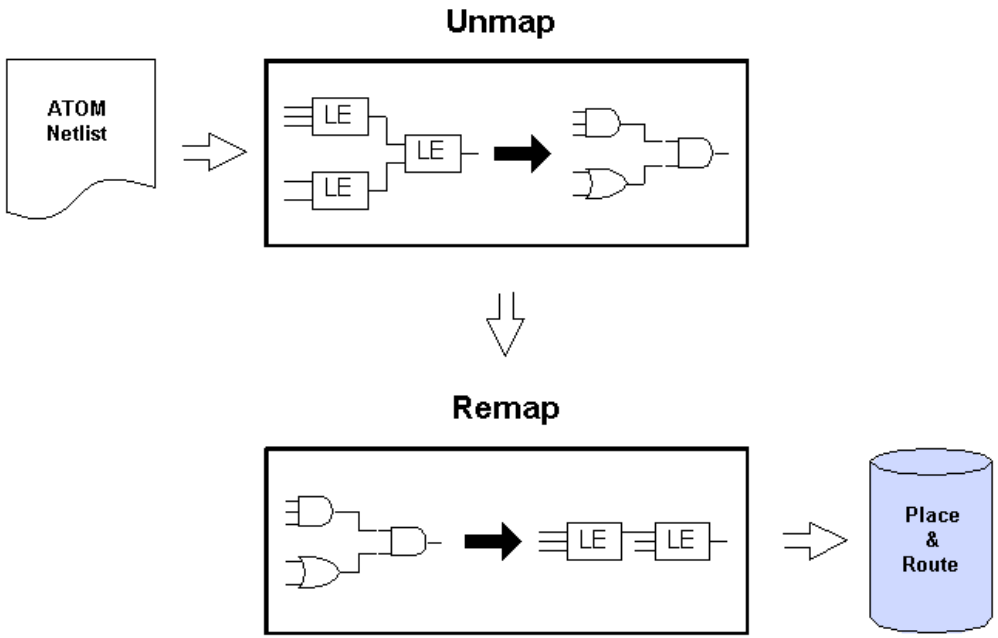
Netlist Optimization Options

- WYSIWYG Primitive Resynthesis
- Gate-level Register Retiming
- Retiming Trade-Off With Tsu/Tco
- Logic Element Duplication



WYSIWYG Primitive Resynthesis

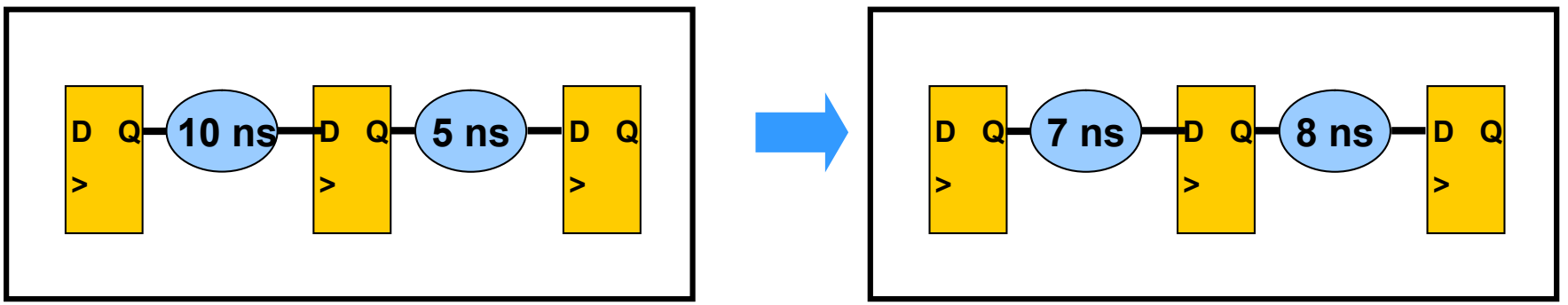
- Used with Atom NetlistfFrom 3rd Party Tool
- Unmaps Altera Primitives to Gates & Then Remaps
- Option Not Available When Using Native Synthesis



Why?

Gate-Level Register Retiming

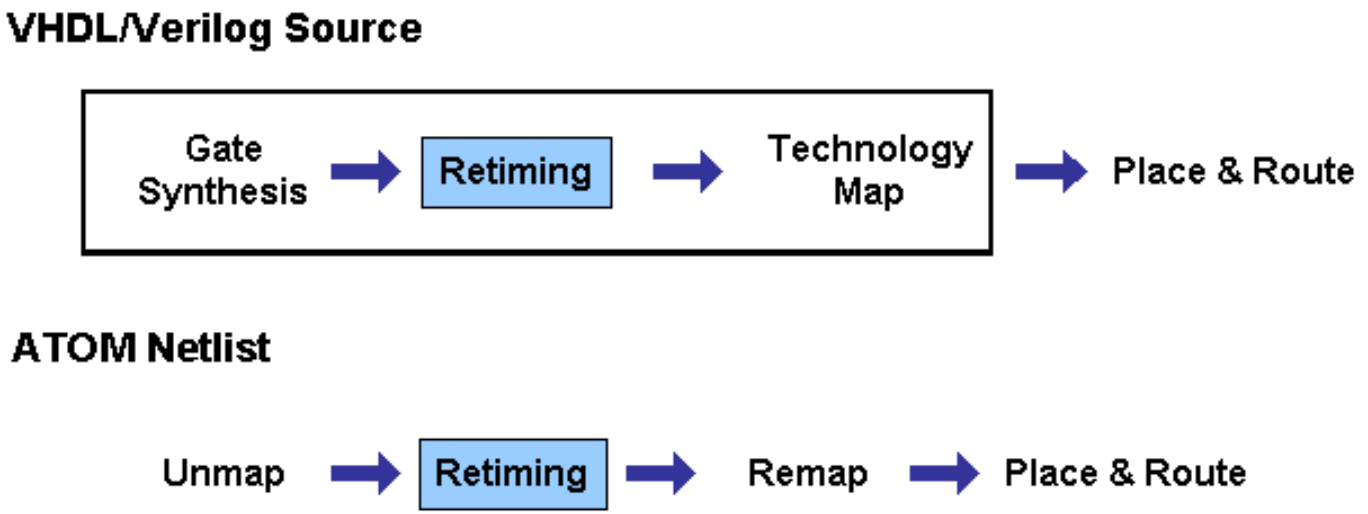
- Moves Registers across Combinatorial Logic to Balance Timing
- Trades off Between Critical & Non-Critical Paths
- Changes at Gate Level



Gate-Level Register Retiming

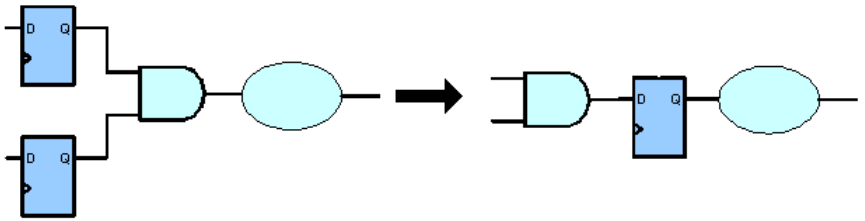
- Must Use WYSIWYG Primitive Resynthesis Option if Using an ATOM Netlist ***Why?***

  Must Happen at Gate Level!



Gate-Level Register Retiming

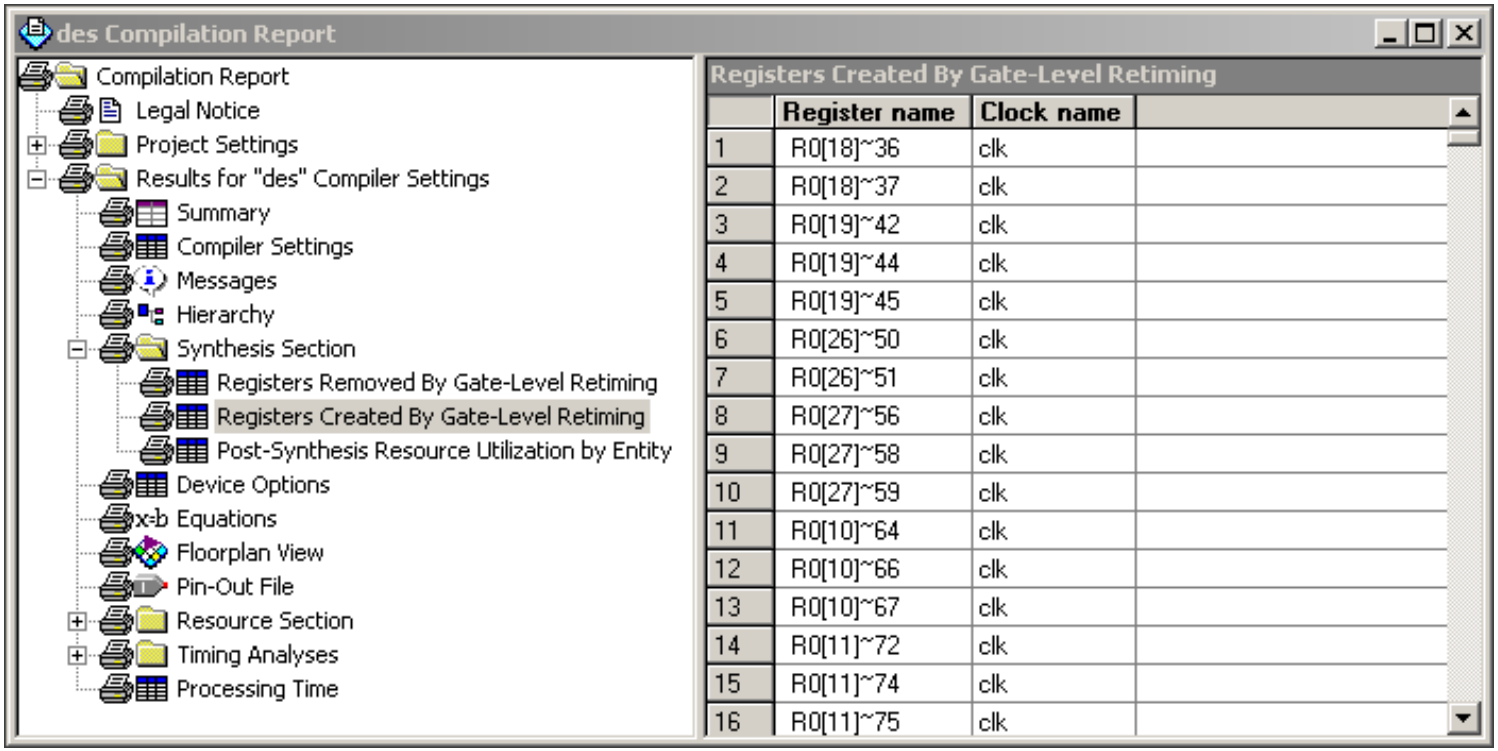
- Options Allows Registers to Be Combined If



  - All Registers Have Same Clock
  - All Registers Have Same Clock Enable
  - All Registers Same Asynchronous Control Signals
  - Only One Register Has Asynchronous Load Other than VCC or GND

Gate-Level Register Retiming

- List of Registers Created & Removed in Compilation Report

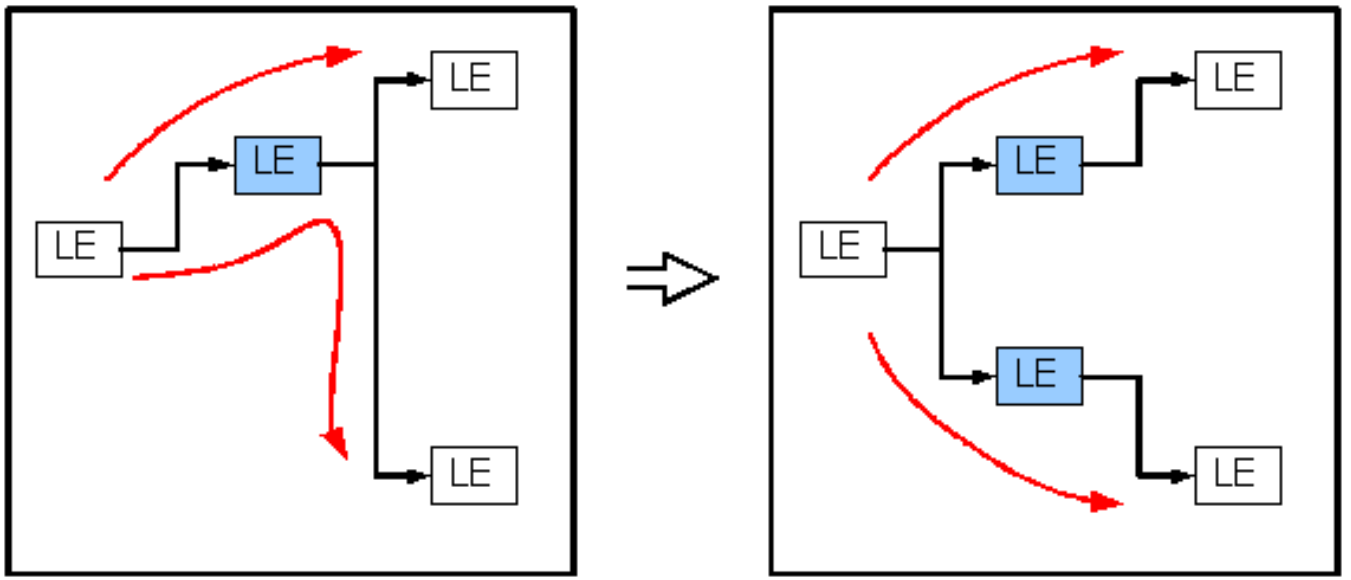


Registers Created By Gate-Level Retiming

	Register name	Clock name
1	R0[18]~36	clk
2	R0[18]~37	clk
3	R0[19]~42	clk
4	R0[19]~44	clk
5	R0[19]~45	clk
6	R0[26]~50	clk
7	R0[26]~51	clk
8	R0[27]~56	clk
9	R0[27]~58	clk
10	R0[27]~59	clk
11	R0[10]~64	clk
12	R0[10]~66	clk
13	R0[10]~67	clk
14	R0[11]~72	clk
15	R0[11]~74	clk
16	R0[11]~75	clk

Logic Element Duplication

- Allows LEs that Fan Out to Multiple Locations to Be Duplicated
- Based on Fitter Information



Netlist Optimization Options

- With Third Party Atom Netlist
  1. No Netlist Optimizations Turned On
  2. WYSIWYG Primitive Resynthesis Turned On
  3. WYSIWYG Primitive Resynthesis & Gate-Level Register Re-timing Turned On
  4. Logic Element Duplication Turned On
  5. All Three Turned On
- Quartus® II Native Synthesis
  1. No Netlist Optimizations Turned On
  2. Gate-level Register Re-timing Turned On
  3. Logic Element Duplication Turned On
  4. Gate-Level Register Re-Timing & Logic Element Duplication Turned On

Design Analysis

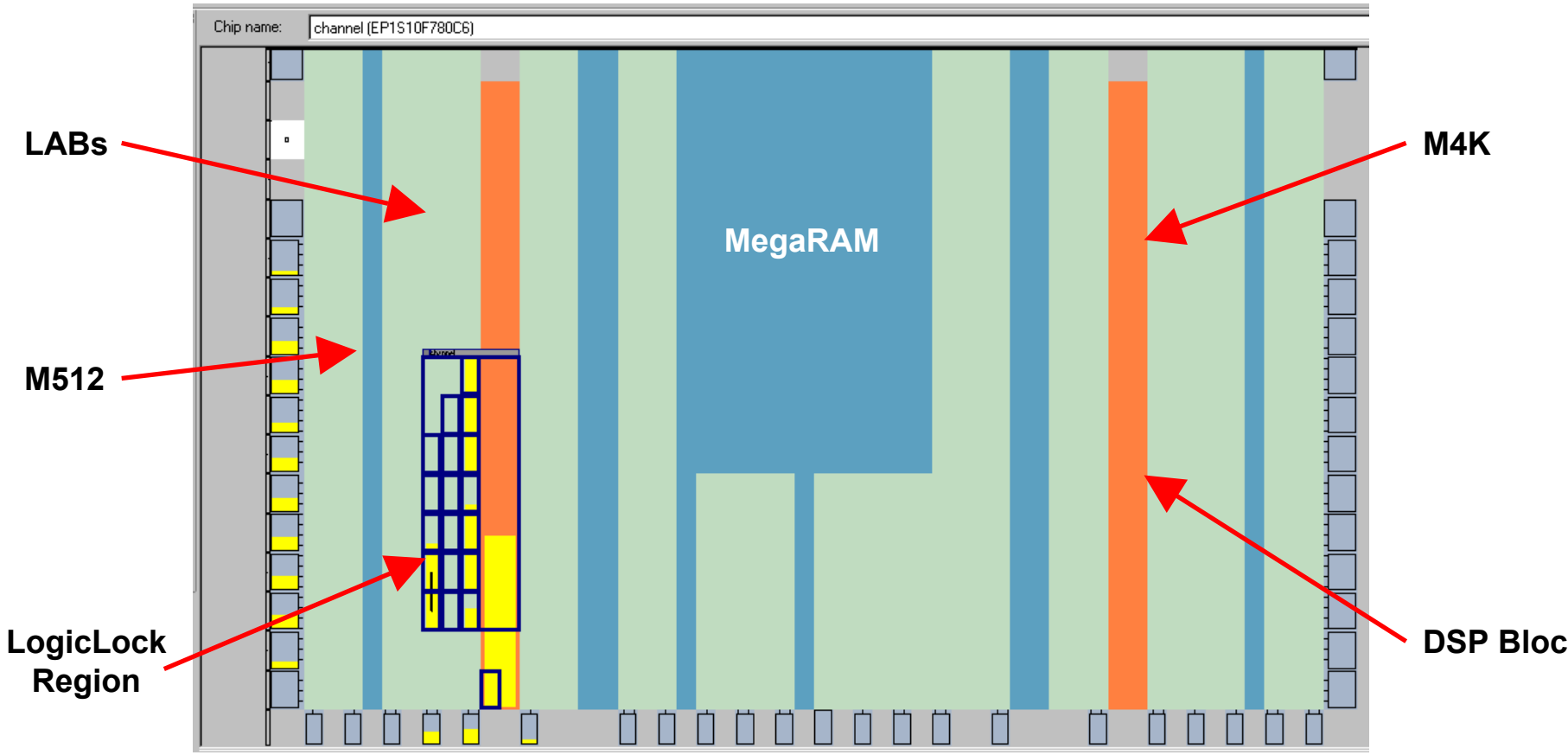
- After Compiling, Need to Analyze Design
- Two Common Ways We Do So
  - Timing Analysis Report
  - Floorplans
    - Current Assignments
    - Last Compilation
    - Timing Closure
- We Will Focus on the New Timing Closure Floorplan

Timing Closure Floorplan

- Floorplan Views
  - Field View *New*
  - Interior Cells
  - Package Top
  - Package Bottom
- Viewing Assignments
- Critical Paths
- Physical Timing Estimates
- LogicLock Region Connectivity

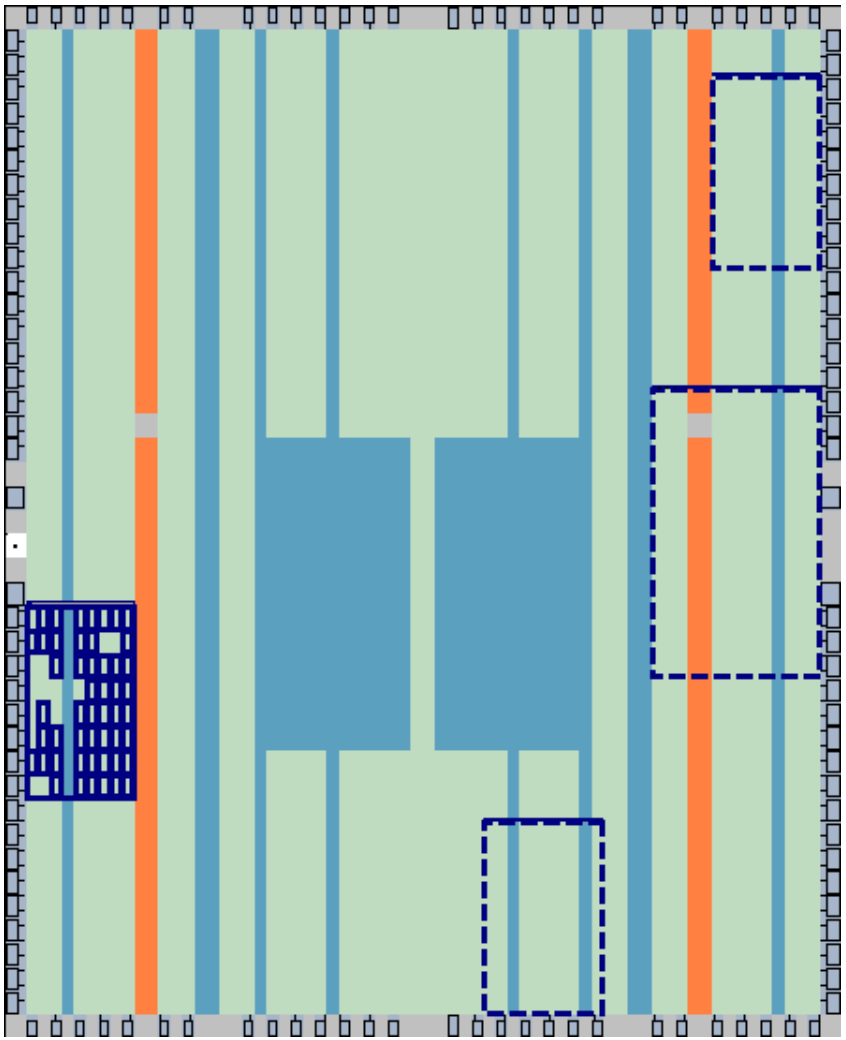
Field View

- Shows Resources



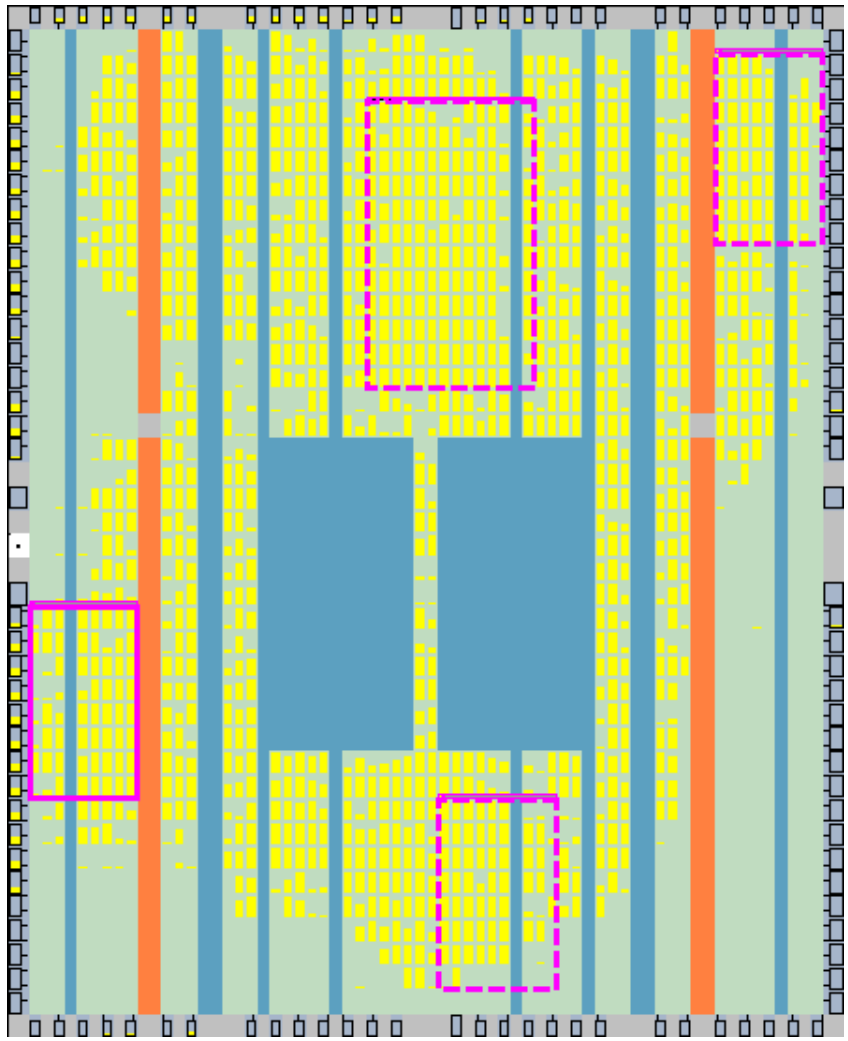
User Assignments

- Displays Current Assignments
- LogicLock Regions Shown in Navy



Fitter Placements

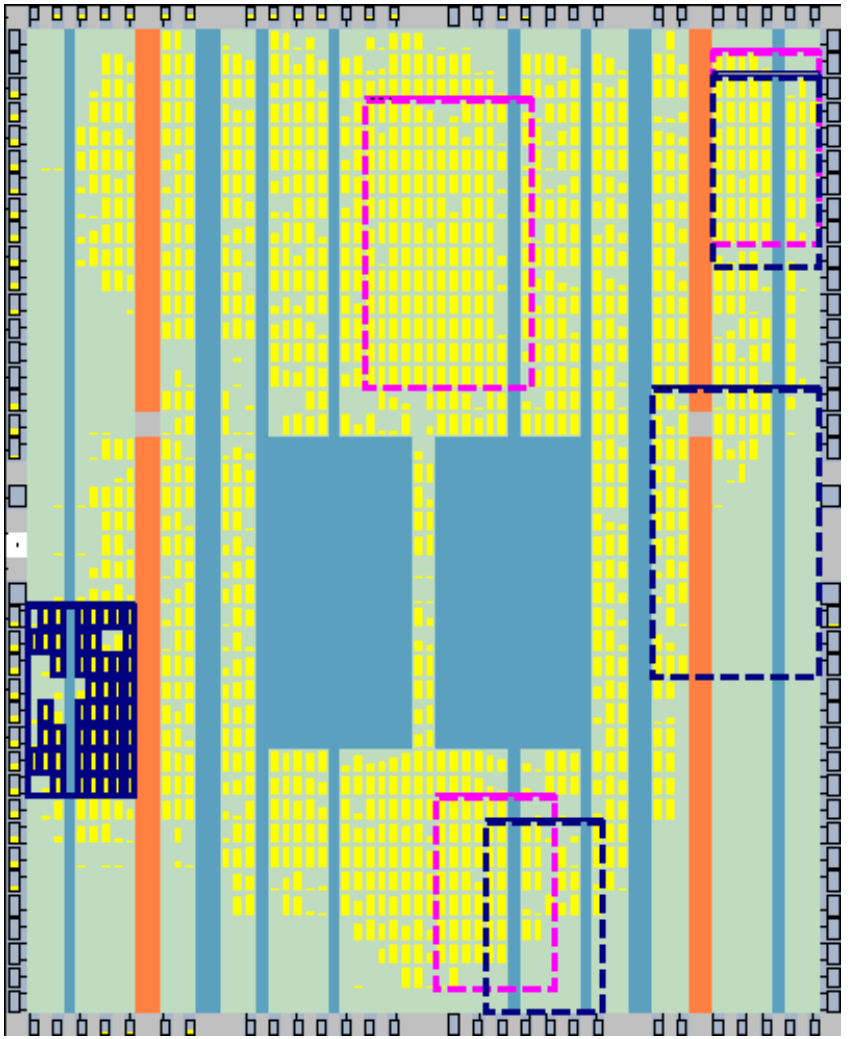
- Displays Last Compilation Assignments
- LogicLock Regions Shown in Magenta



Viewing Assignments

- Can View User Assignments & Fitter Locations Together

Why Different Region Locations?



Critical Paths

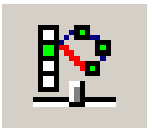
- New Utility in Quartus II
- View Paths with Longest Delay
- Can Choose to View
  - A Number of or Percentage of Critical Paths
  - Paths in All Clock Domains or a Specific Clock Domain
  - Type of Paths

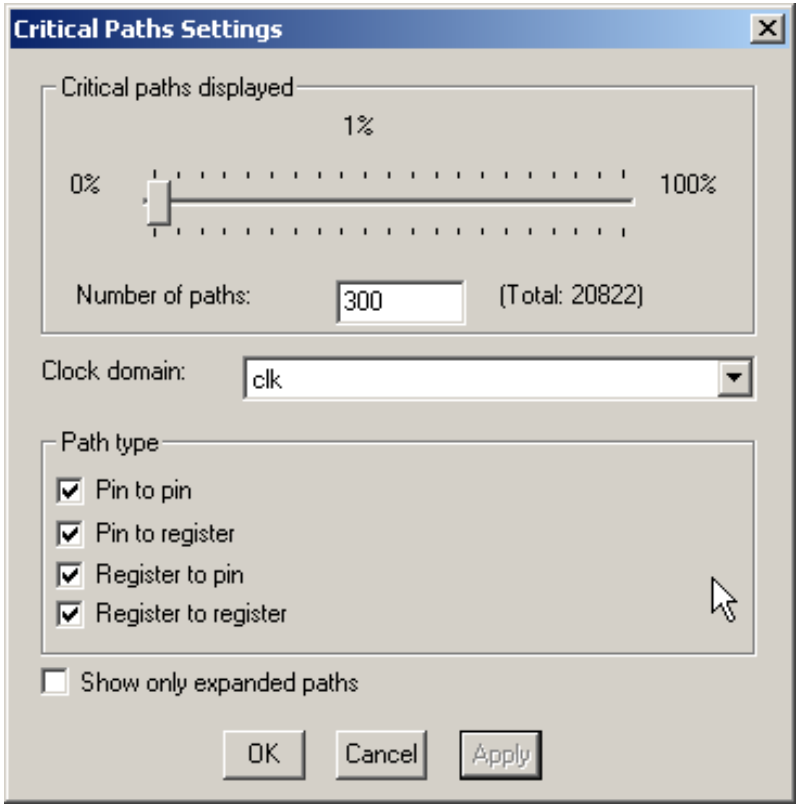
What Do These Types Mean?

- Pin-to-Pin t_{PD}
- Pin-to-Register t_{SU}
- Register-to-Pin t_{CO}
- Register-to-Register F_{MAX}

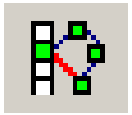
Critical Path Settings Window

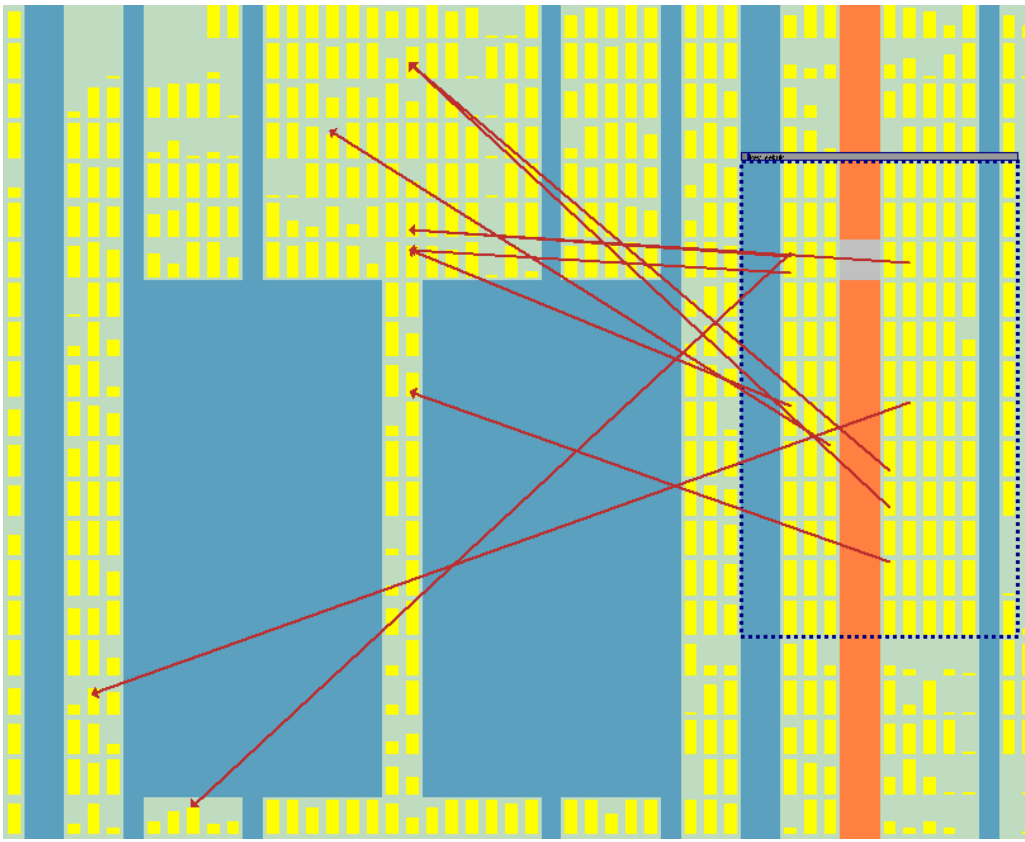
- View -> Routing -> Critical Path Settings
- Critical Path Settings Icon





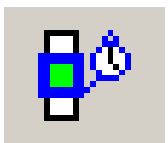
Critical Paths

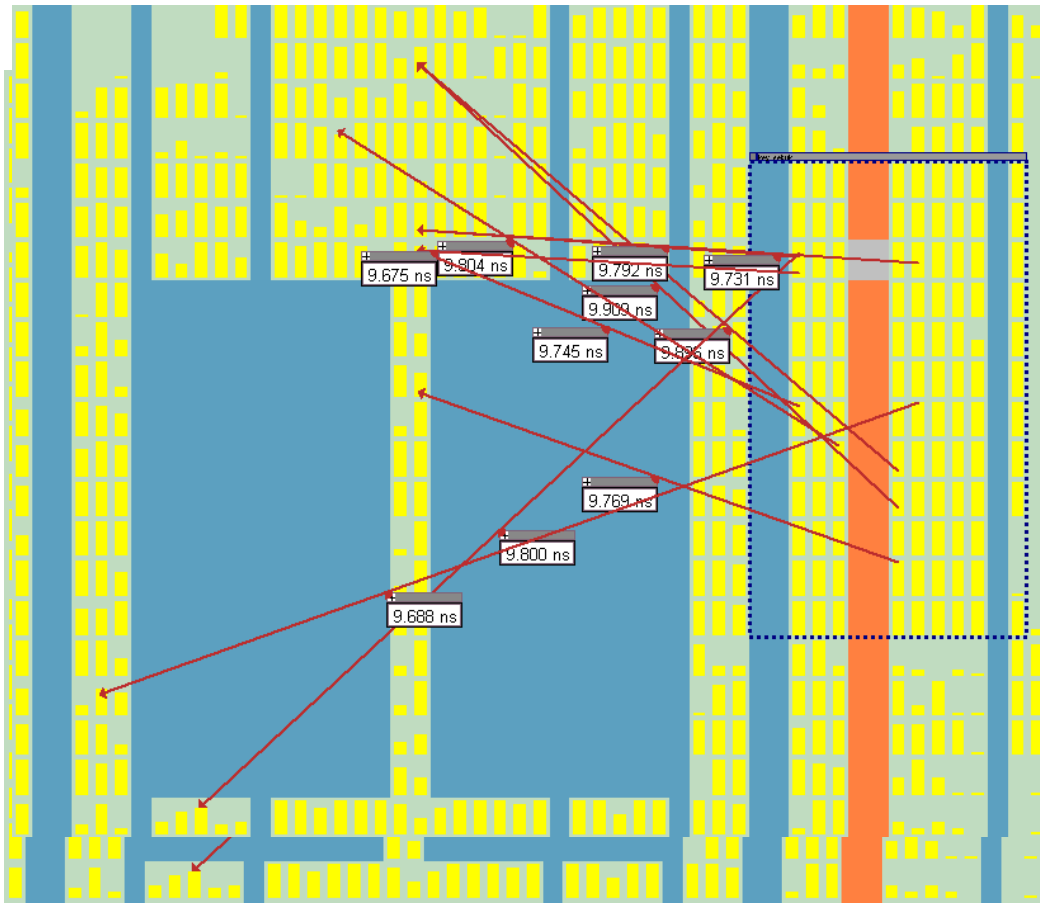
- View -> Routing -> Show Critical Path
- Show Critical Paths Icon 



Critical Path Routing Delays

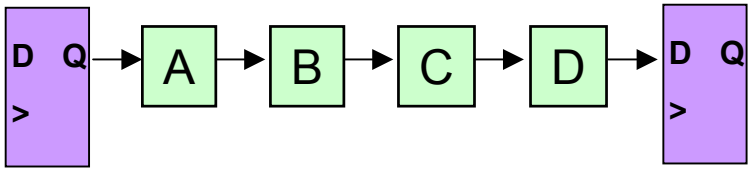
- Can View Routing Delay of Critical Paths
- View -> Routing -> Show Routing Delays
- Show Routing Delays Icon





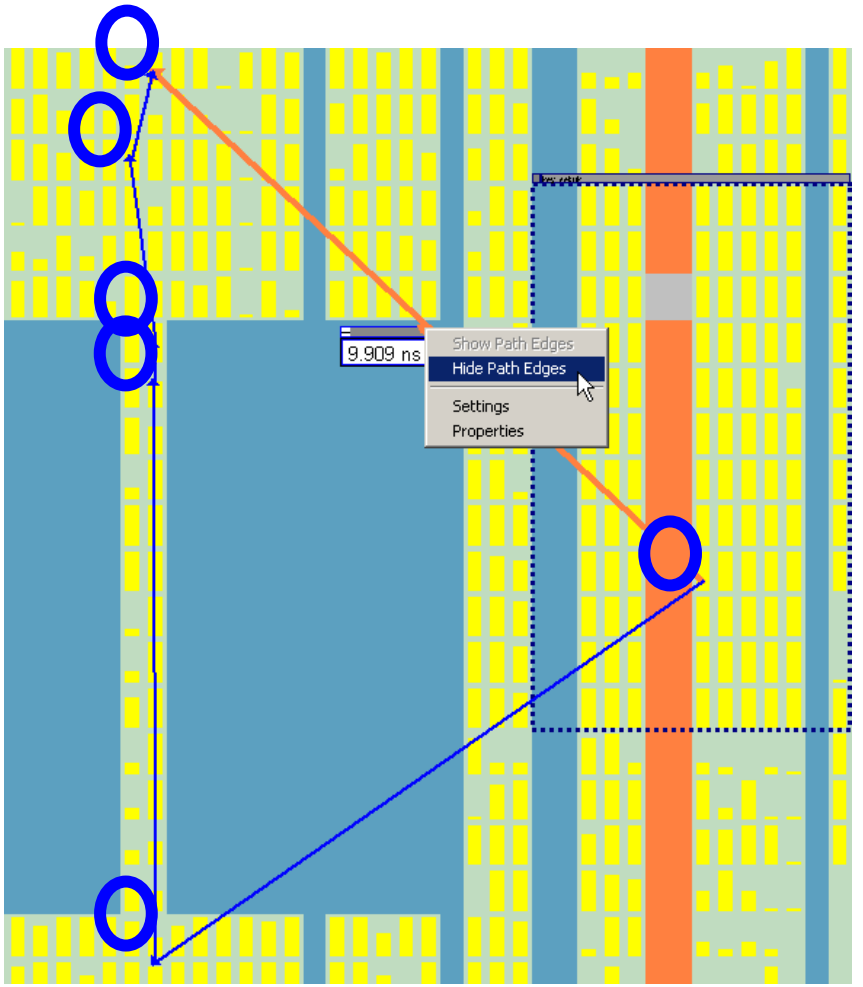
Show Path Edges

- Shows Worst Case Path Between Registers



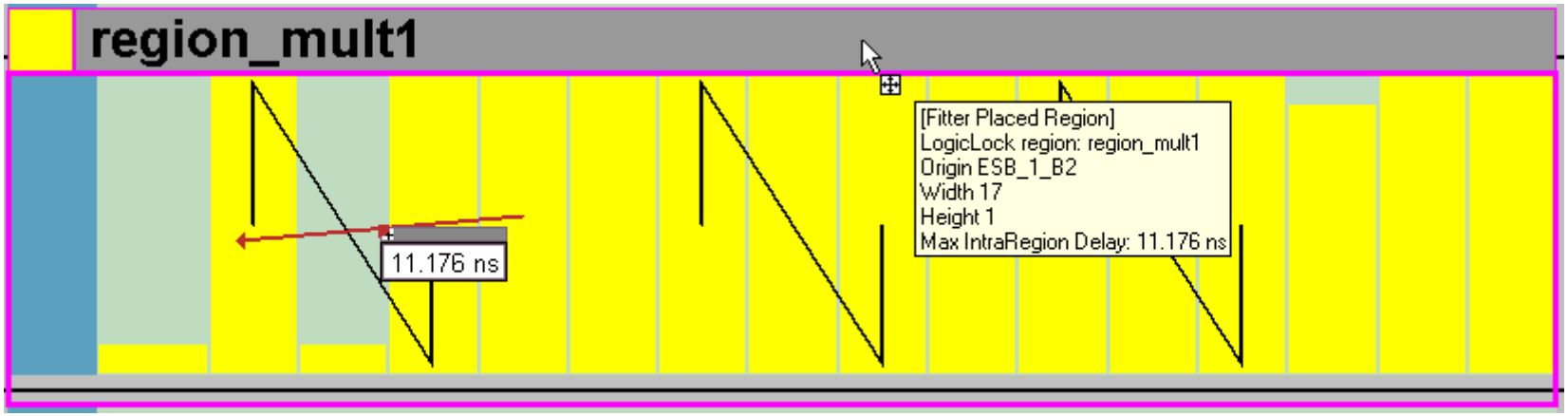
Source

Destination



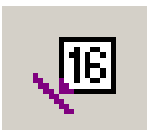
Max IntraRegion Delay

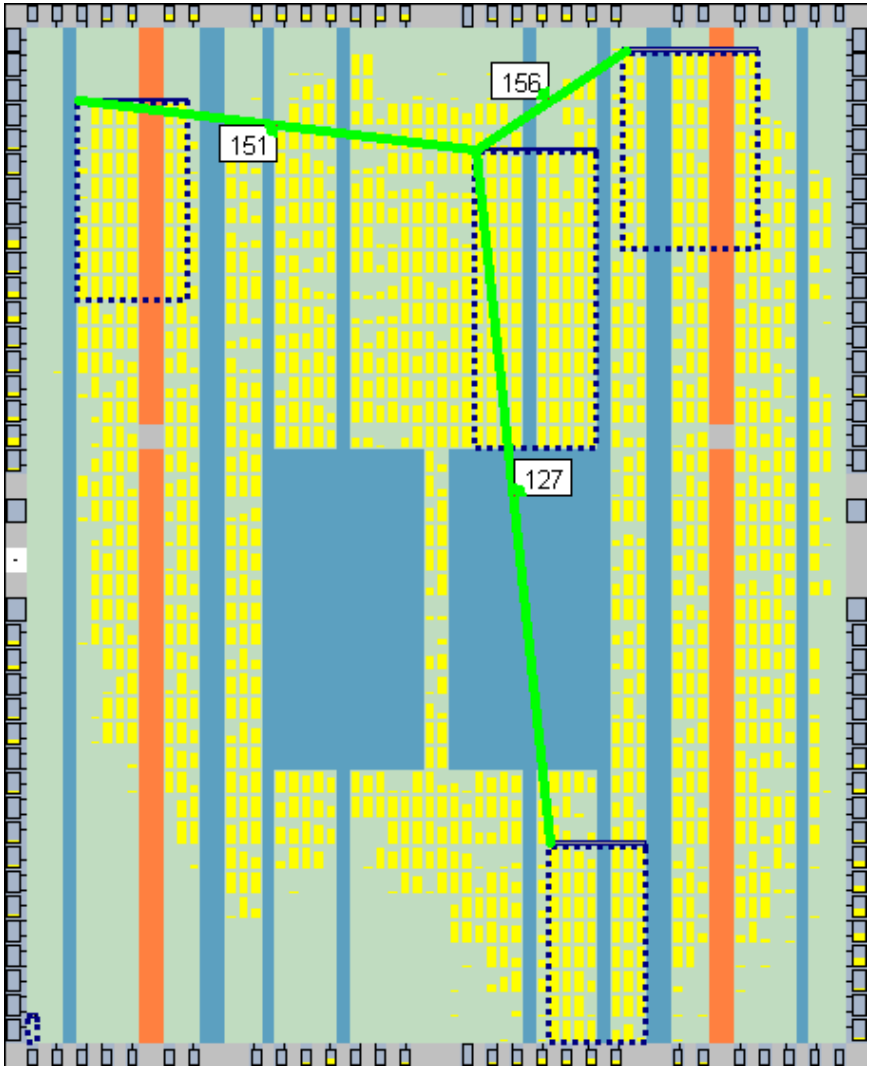
- Available After Using the Critical Paths Utility Once
- Put Mouse Over LogicLock Region Handle
- Maximum Delay Possible in LogicLock Region



LogicLock Region Connectivity

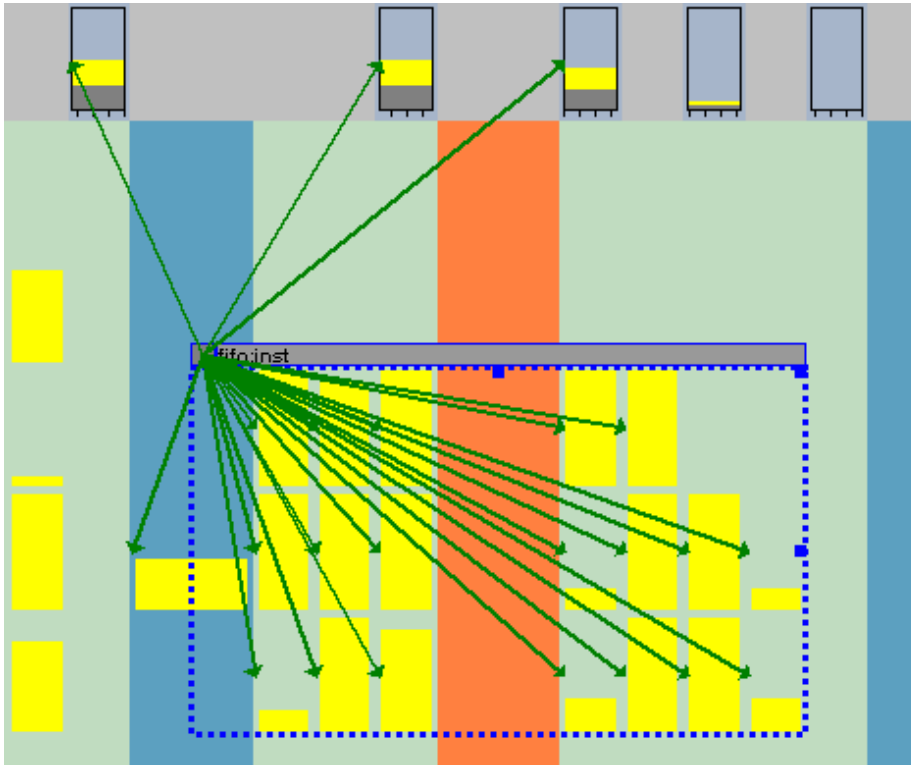
- Number of Connections Seen With Thickness of Line
- To See Number of Connections, Select Show Connection Count Icon





LogicLock Region Fan-In/Fan-out

- Can See Fan-in & Fan-out of Regions
- Only Nodes with User Assignments Will Be Shown



Timing Closure Assignments

- Quartus II Assignments
  - Location Assignments
  - LogicLock Regions
- Applying Assignments
  - Node Assignments
  - Entity Assignments
  - Path-Based Assignments

Location Assignments

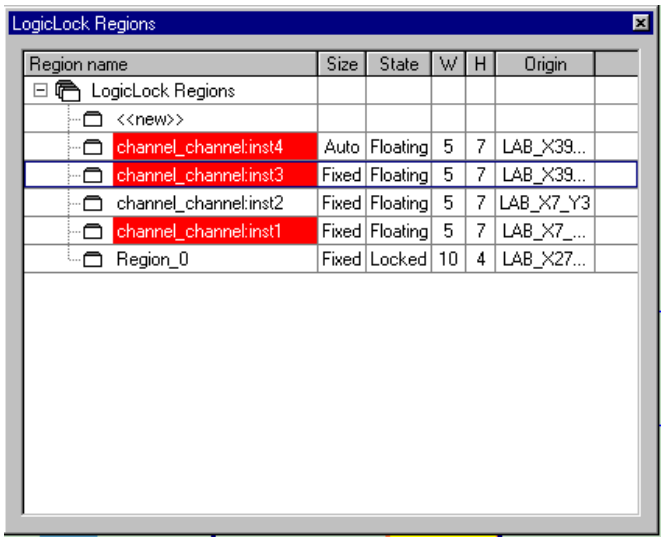
- Hard Assignments of Nodes to Resources
  - Logic Elements
  - Memory Blocks
  - DSP Blocks
- Can Do Through
  - Assignment Organizer
  - Current Assignments Floorplan
  - Timing Closure Floorplan

LogicLock GUI

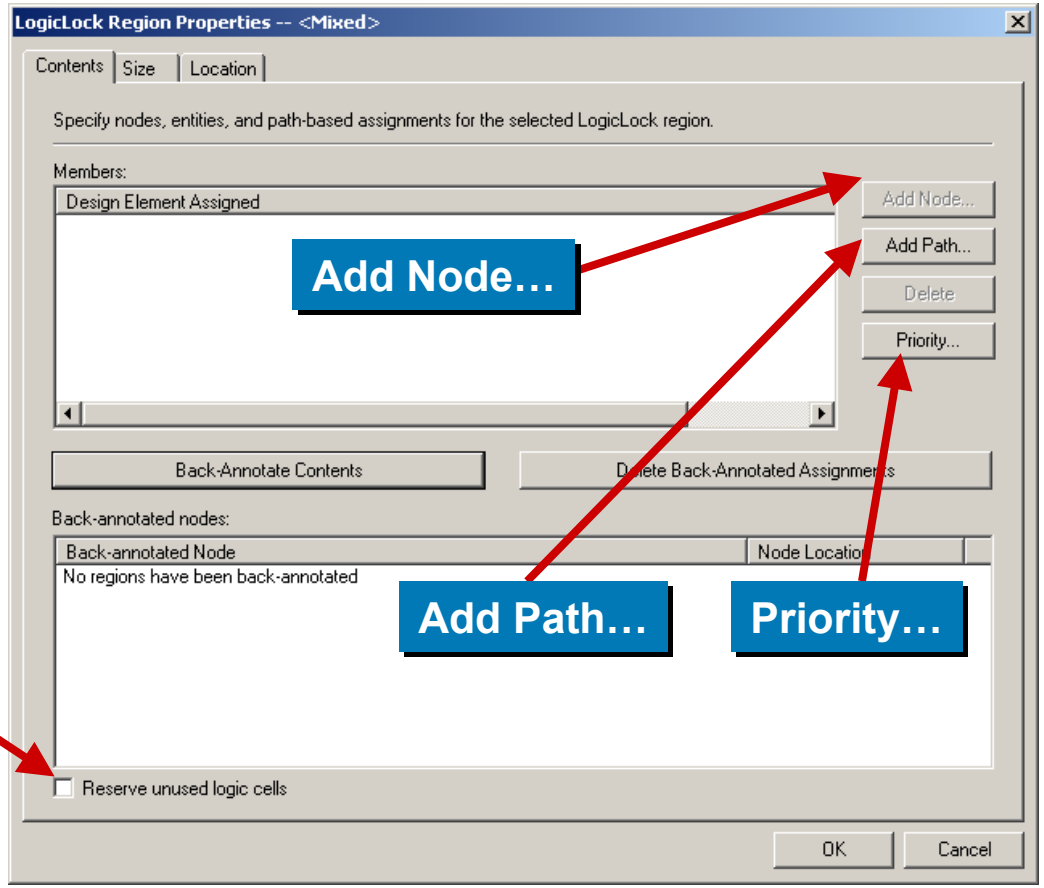
- Quartus II 2.1 Introduces New View for LogicLock
- Comprised of 2 Dialog Boxes
  - LogicLock Regions
  - LogicLock Region Properties
- Tabular, Editable Display of Properties
- Column Display Is Configurable
- Regions with Invalid Properties Shaded Red
  - Repair Region via Context-Menu Entry

LogicLock GUI

LogicLock Regions



LogicLock Region Properties

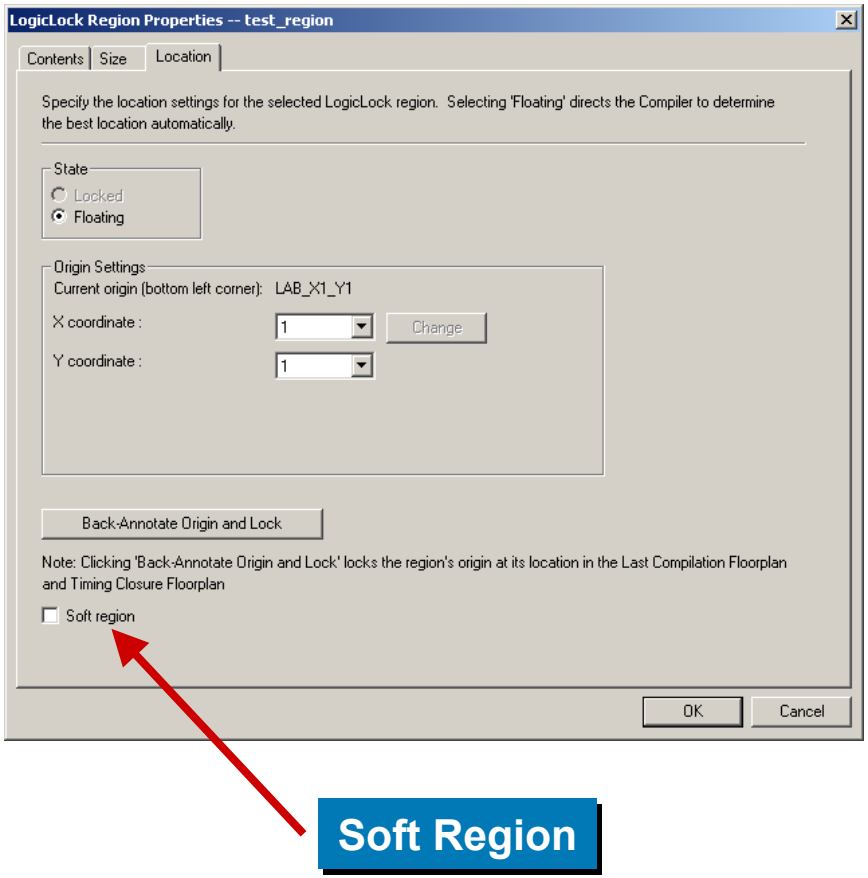


Creation Of LogicLock Regions

- Quartus II Version 2.1 Provides 4 Methods to Create LogicLock Regions
  - Using The LogicLock Regions Dialog Box
  - Using The Floorplan Editor
  - Using The Hierarchy Window
  - Using A Tcl Script

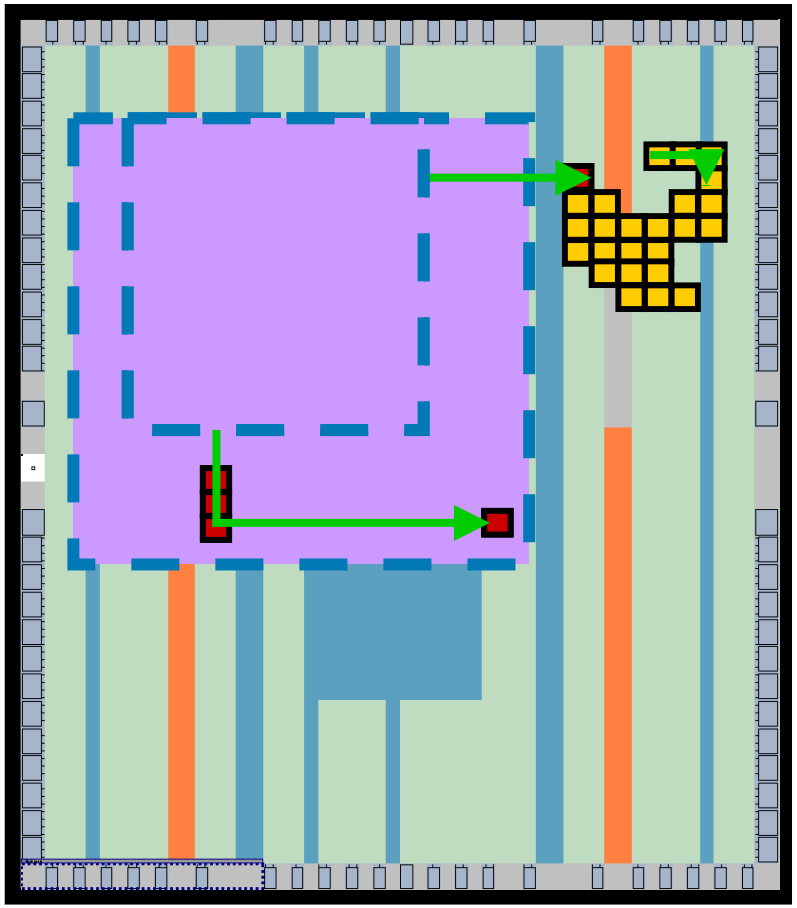
Soft LogicLock Regions

- LogicLock Regions Are Defined With A Hard Rectangular Boundary
- Soft LogicLock Regions Removes The Hard Boundary
  - Quartus II Has The Ability to Remove Nodes Within a LogicLock Region That Has Been Declared Soft



Soft LogicLock Regions

- An Arbitrary Hierarchy Can Be Applied to Soft LogicLock Regions
- Soft LogicLock Regions Will Remain Within The Boundaries of The First Non-Soft Region



Node Assignments

- Nodes Are Altera Specific Primitives
- Can Be Made Through
  - Assignment Organizer
  - Current Assignments Floorplan
  - Timing Closure Floorplan
  - Back-annotating Design

Entity Assignments

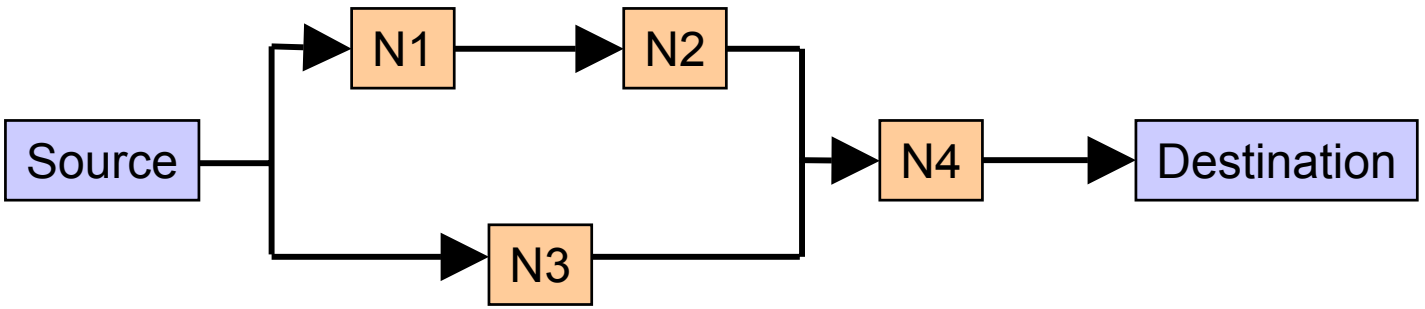
- Modules of a Design
- Can Be Made Through
  - Assignment Organizer
  - Dragging and Dropping From Hierarchies Window to
    - Timing Closure Floorplan
    - LogicLock Regions Window

Path-Based Assignments

- Can Only Be Made to LogicLock Regions
- Can Be Made:
  - Using New Path Window
  - By Dragging and Dropping Paths From Timing Analysis Section of Compilation Report
  - By Dragging and Dropping Using the Critical Paths Utility in the Timing Closure Floorplan

Path-Based Assignments

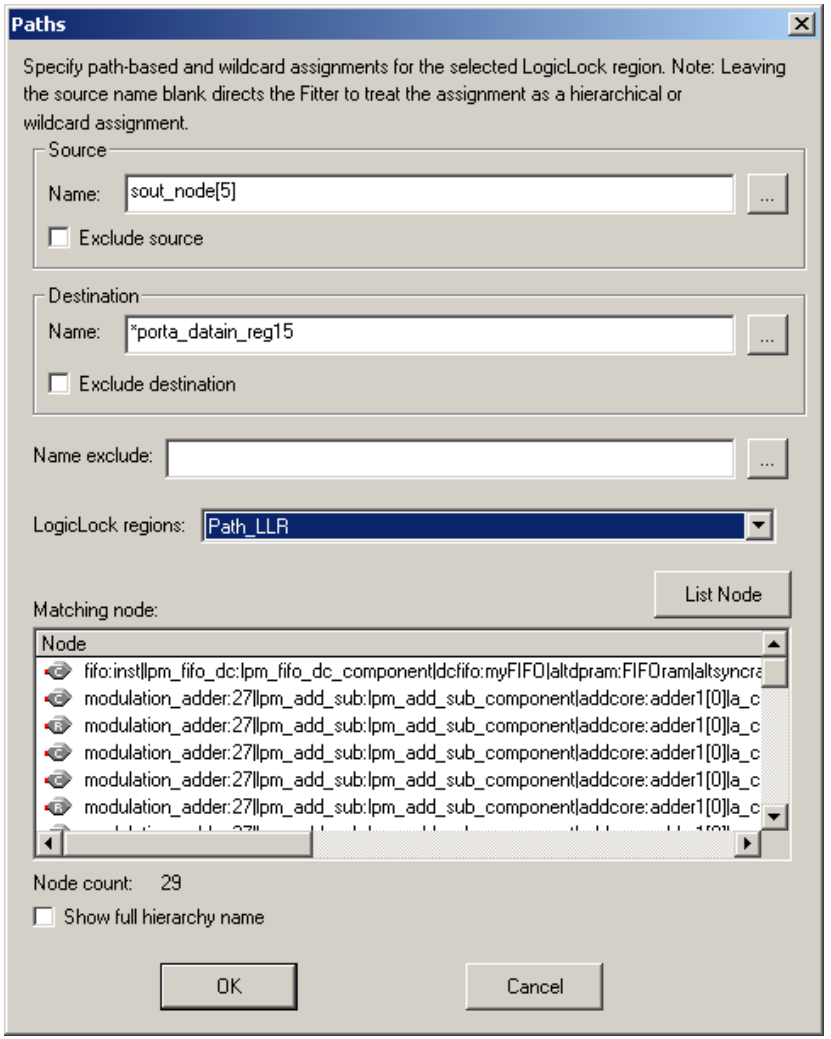
- Assigns Every Path From Source & Destination Nodes
  - Nodes Source, N1, N2, N3, N4, Destination Will Be Assigned



What Nodes Shown If Using Critical Paths?

Path Window

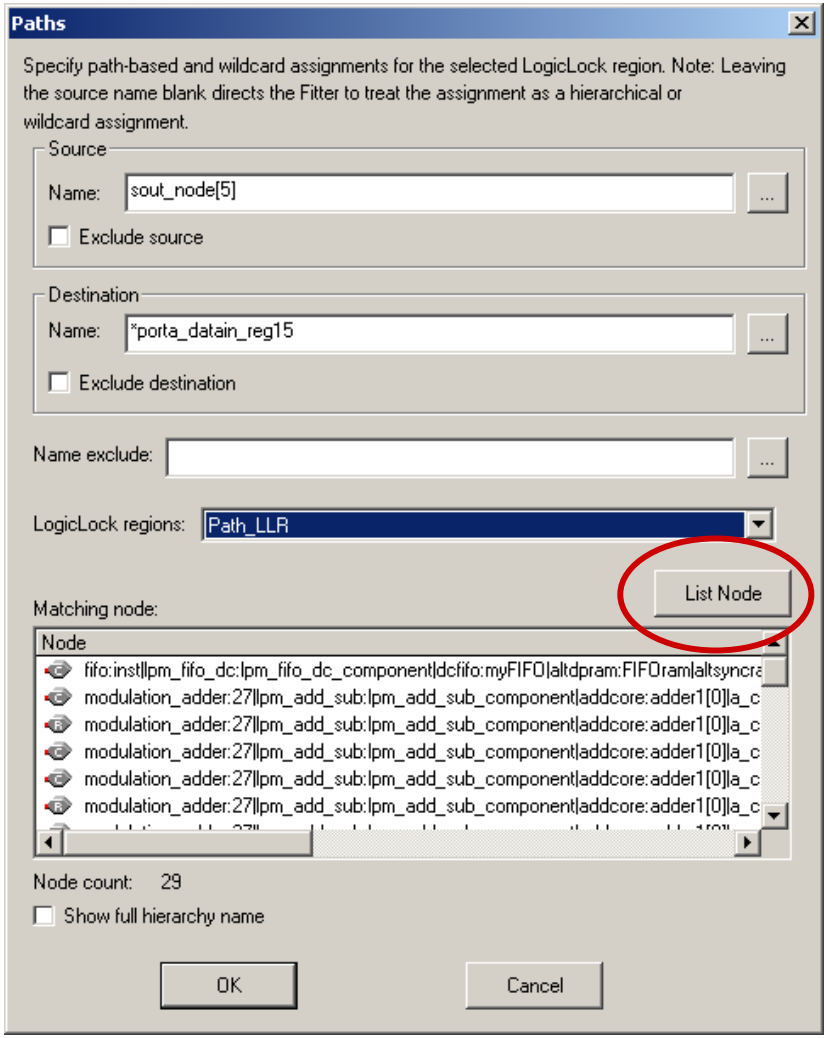
- Allows Path to Be Specified Using Source & Destination
- Can Exclude Nodes
  - Source
  - Destination
  - Matching Wildcard
- Can Change LogicLock Region



Path Window

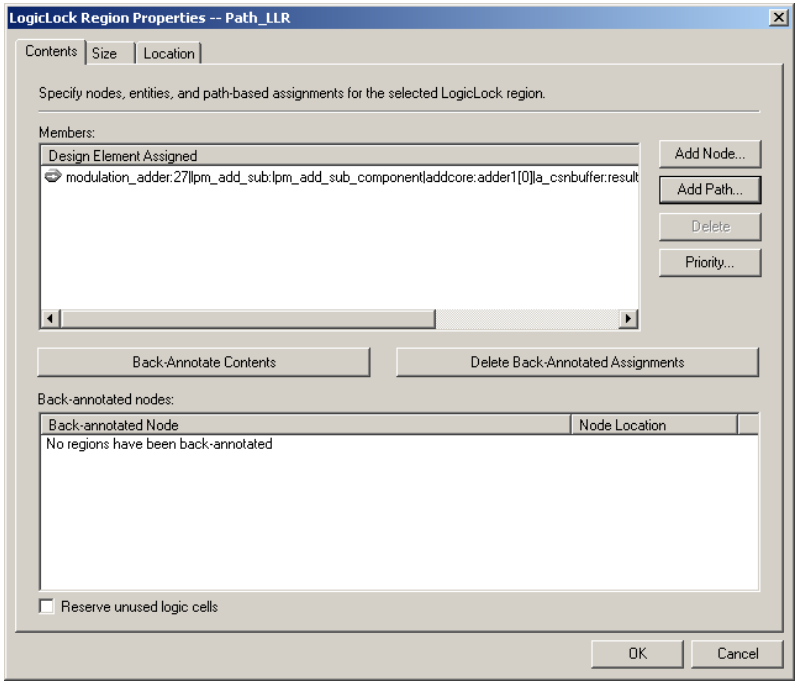
- List Node Lists Every Node to Which Assignment Will Apply
- Can Use * & ? Wildcards in
  - Source Name
  - Destination Name
  - Name Exclude

What Does * Wildcard Do?
What Does ? Wildcard Do?

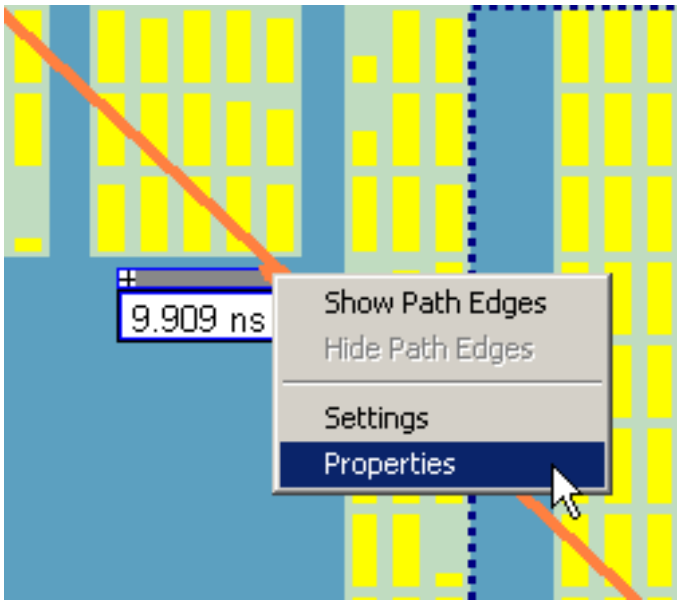


Path Window

- Can Access Path Window from



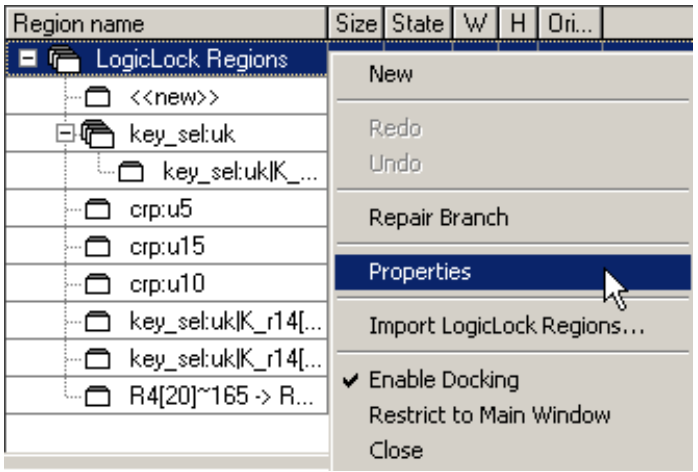
LogicLock Regions Properties Window

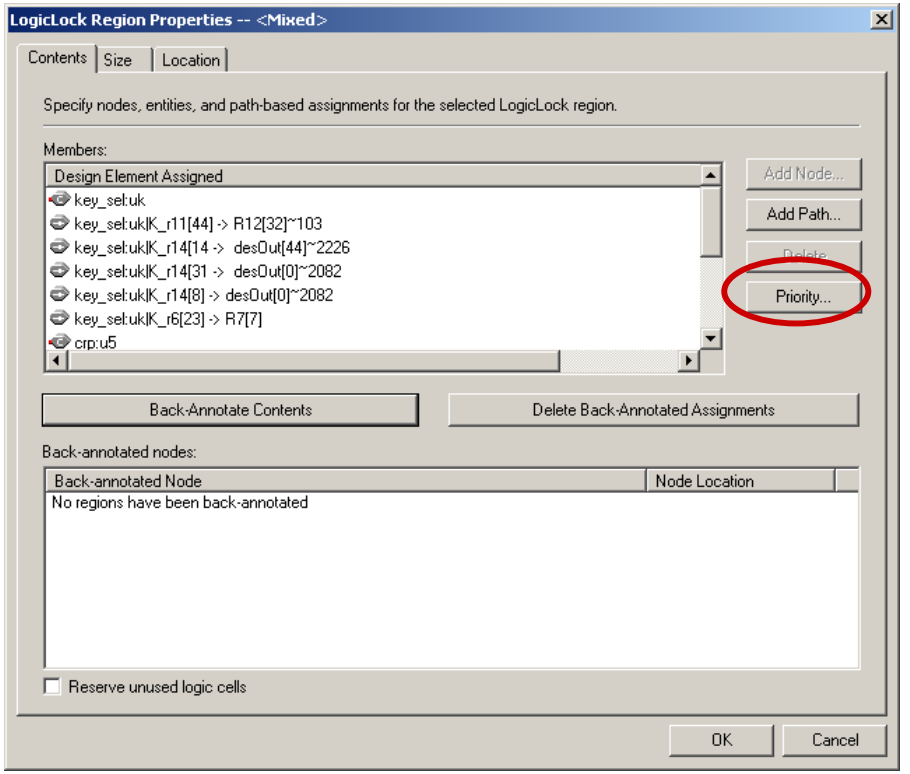


Right Clicking on Critical Path

Priority of Assignments

- Need Way to Determine Priority of Nodes Assigned through Paths or Wildcards
- Priority Window





Summary

- New Integrated Synthesis
- Now a Detailed Timing Closure Flow
- Netlist Optimization Options Available
- New Timing Closure Floorplan Tools for Design Analysis
- Making Assignments to Achieve Timing Closure