SOPC WORLD 2002

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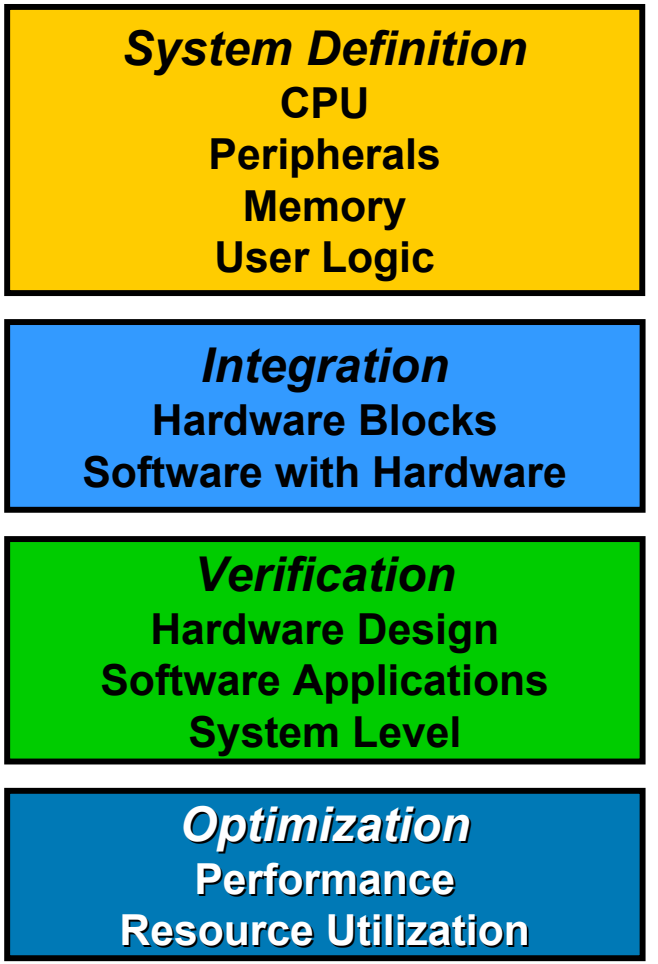
Hardware/Software Co-Design in Programmable Logic

ALTERA.

Embedded System Development

- Challenges at Every Stage
  - Specification of Hardware & Software Components
  - Integration of Hardware Modules
  - Integration of Software with Hardware
  - Verification of Hardware Functionality
  - Verification of Software Running on Hardware
  - Meeting System Performance Requirements

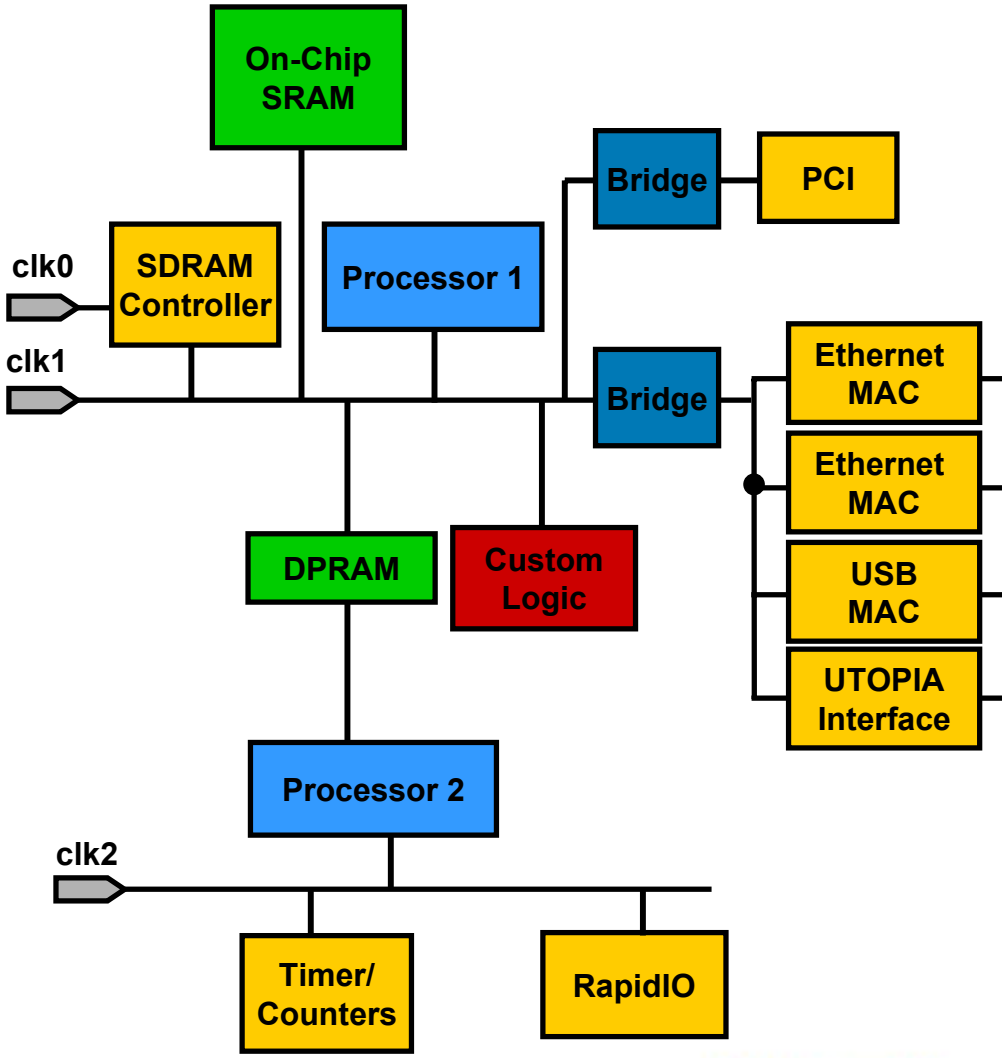


Specification Challenges

- System Component Selection
  - Finding Microcontroller with Exactly the Right Peripherals for Your Application
- Changing System Specification
  - Supporting Leading-Edge Emerging Standards Means High Potential for Changes
  - Feature Creep by Marketing Introduces New Challenges

Hardware Integration Challenges

- IP Block with Different Bus Interfaces
  - Complex Bus Structure
  - Multiple Bus Standards
  - Learning New Specifications
    Impacts Development Time
- Multi-Master & Multi-Slave Systems
  - Arbitration Schemes
  - Decoders
- Multiple Clock Domains
  - Performance Requirements
  - Synchronization When Traversing Domains
- Integration of Custom Logic



Software Development Challenges

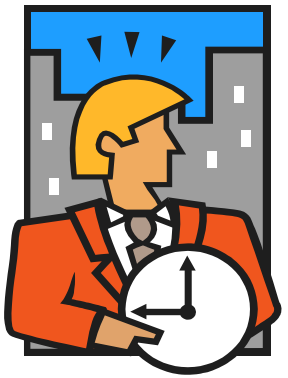
- Accelerating Software Development Cycle
  - Software Development Stalled Waiting for Silicon Prototype
  - Need Hardware or Model to Serve As Virtual Prototype
- Keeping Software Blocks in Sync with Hardware
  - Header Files
  - Peripheral Drivers
  - Software Libraries
  - OS/RTOS Kernels

Hardware/Software Coherency

- Hardware Changes & Software Breaks
  - Hardware Updates
  - Bug Fixes
  - Memory Map Changes
- Updating Header Files & Drivers
  - Error-Prone
  - Tedious
  - Yet Critical to Successful Design

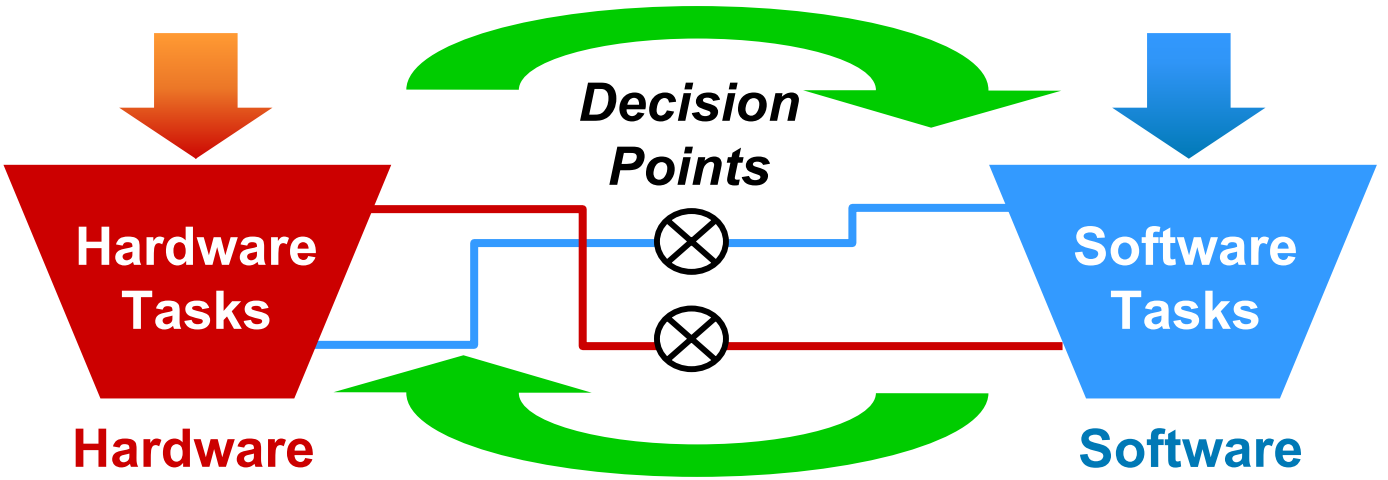
System Verification Challenges

- Increased System Complexity
  - System Level Designs on Single Chip
- Larger Software Content
  - Software IP
  - RTOS
- Need Fast, Effective Way to Validate Complete System
- RTL Models for Hardware
  - Processor Hardware Models Are Slow
  - No Link to Software Debugger
- Test Bench Creation
  - Difficult to Create Hardware & Software Test Bench for IP
    - IP Expertise Lies with Vendor



Meeting System Performance

- Function Too Slow in Software?
  - Implement in Hardware Logic
- Need More Hardware Resources?
  - Implement Non-Time-Critical Functions in Software

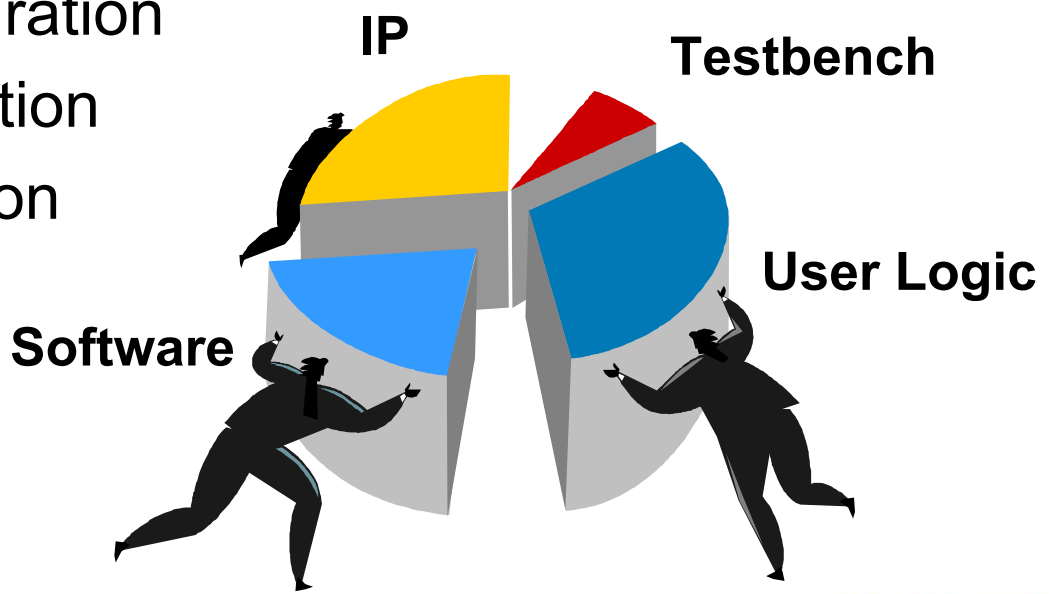


Hardware
- Algorithms
- Devices (ASSP/ASIC/PLD)
- Gates
- Board Area

Software
- Algorithms
- MIPS
- Processor MHz
- Memory Requirements

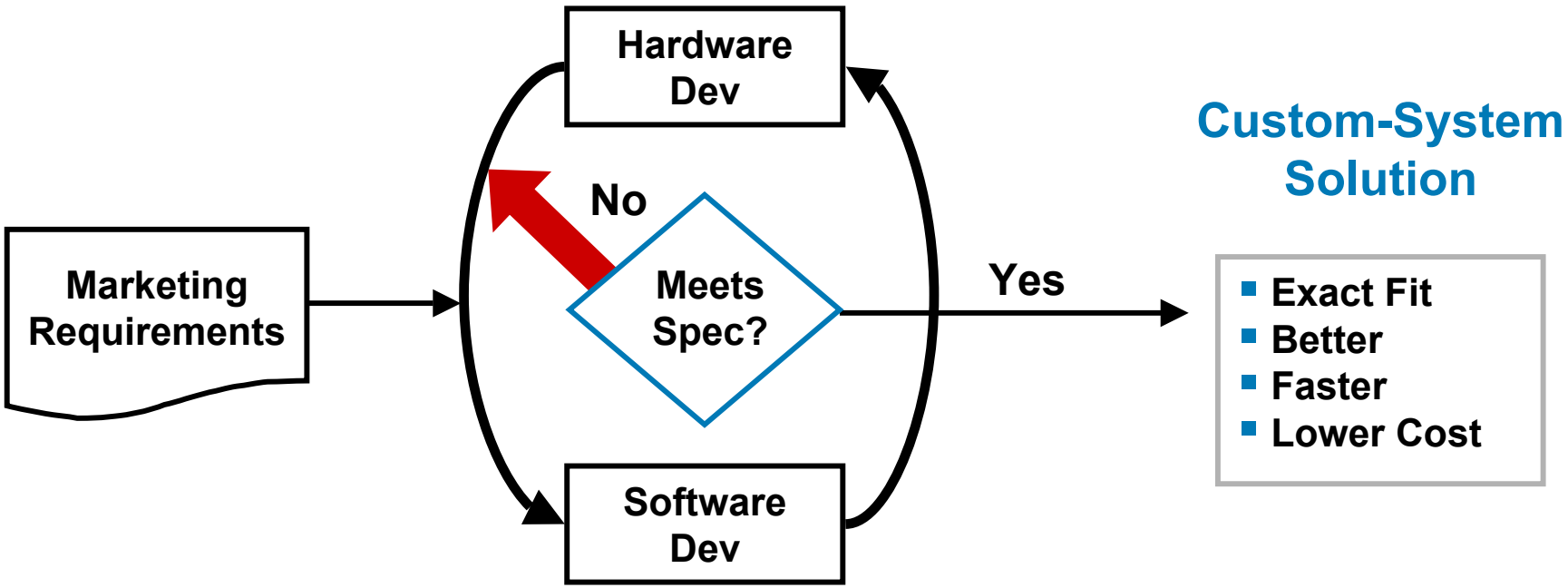
Addressing the Challenges

- Programmable Logic for Rapid Prototyping
- Excalibur™ Embedded Processor Solutions
- SOPC Builder
  - System Customization
  - Component Integration
  - Software Generation
  - System Verification



Hardware/Software Co-Design

- Increase Performance
- Jumpstart Software Development
- Reduce Cost
- Maintain Hardware/Software Coherency



Embedded System Development

- Challenges at Every Stage
  - Specification of Hardware & Software Components
  - Integration of Hardware Modules
  - Integration of Software with Hardware
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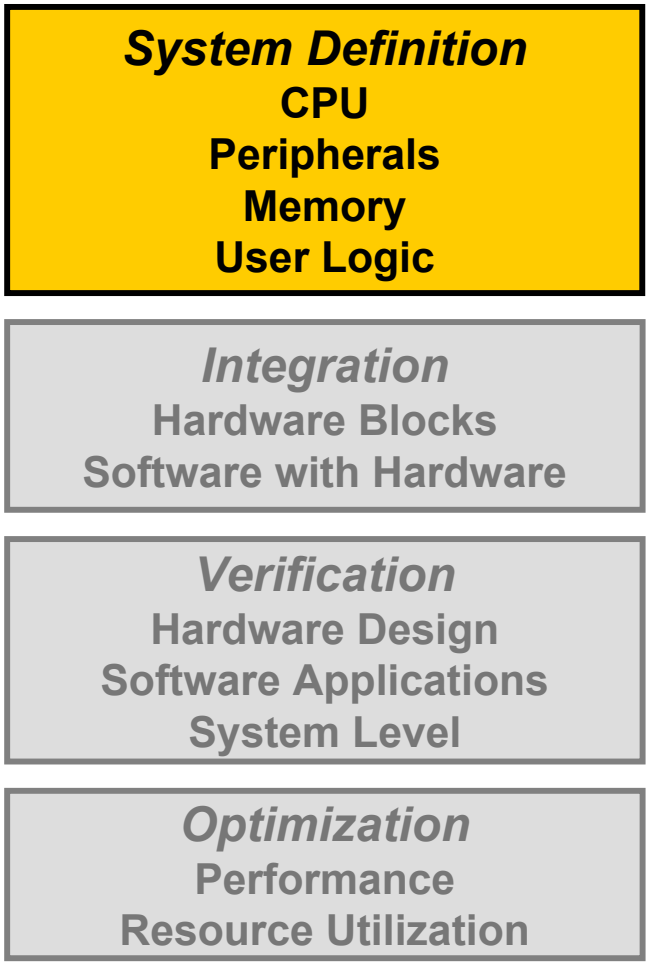
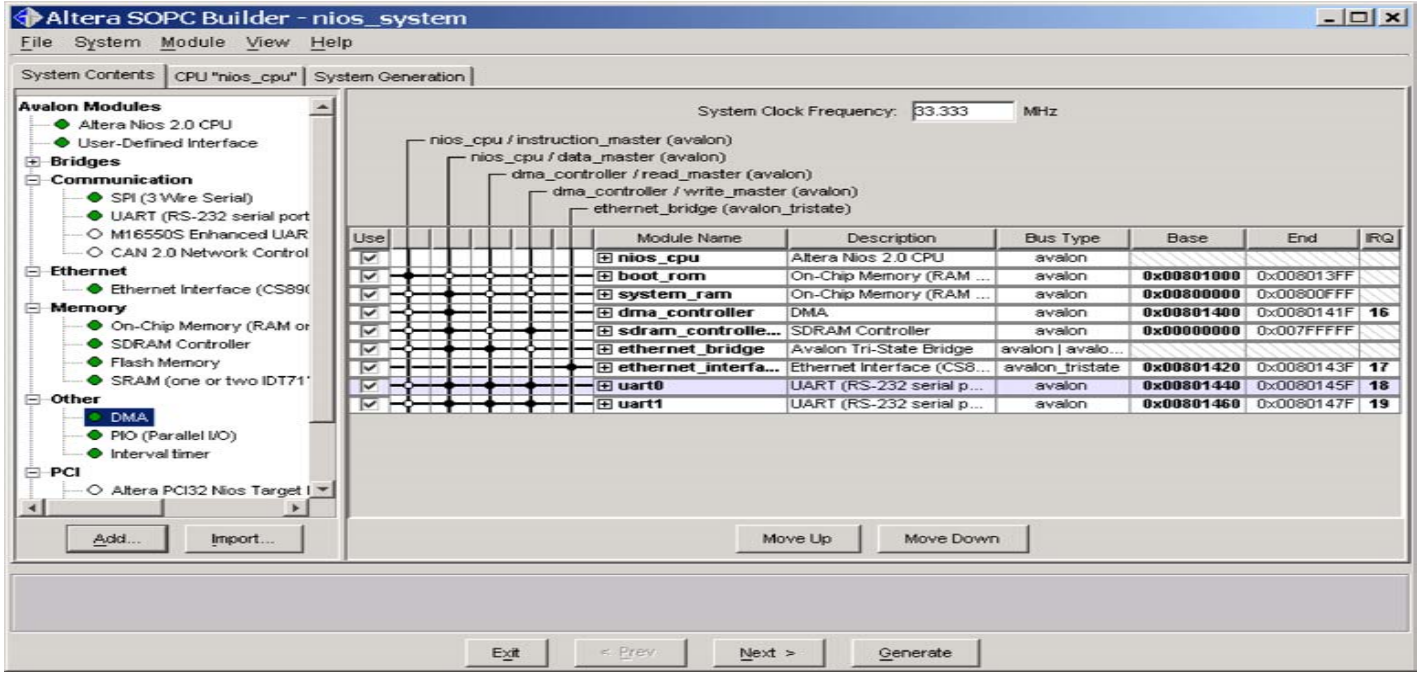


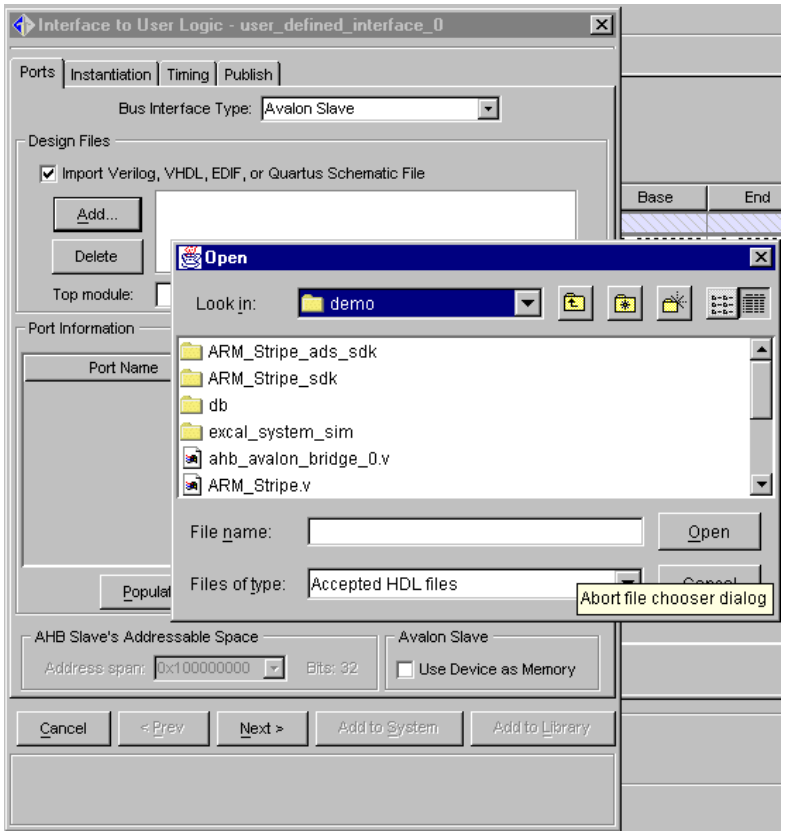
SOPC Builder

- **Exact-Fit Custom Solution**
  - Select From Library of Peripherals
  - Integrate Custom Logic
- **System Changes**
  - Adding New Features
  - Bug Fixes
  - Memory Map Changes

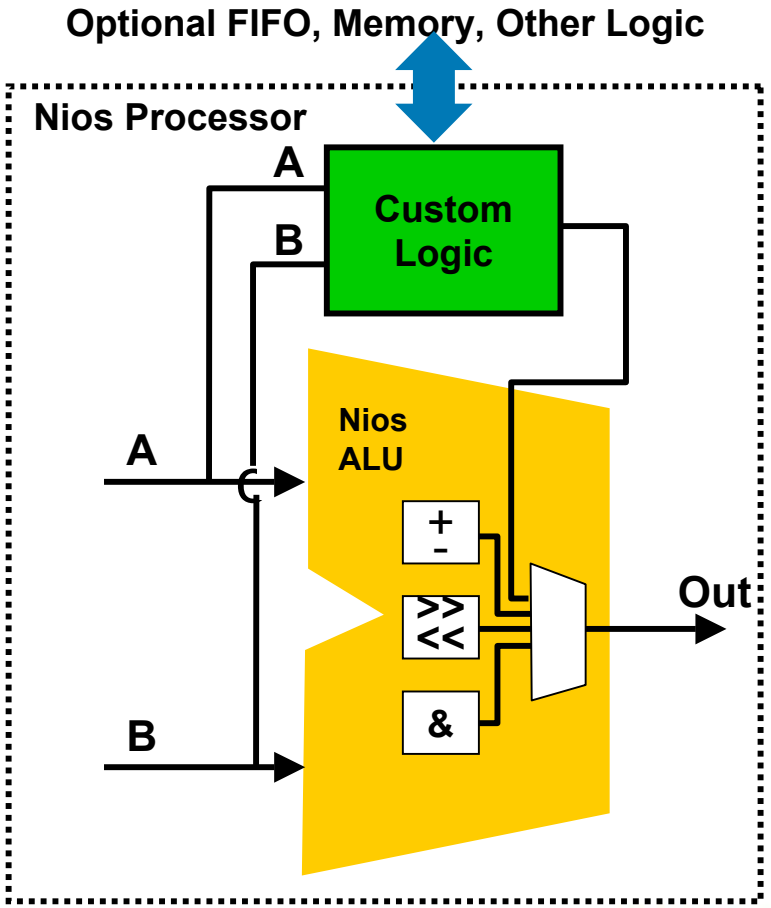


System Customization

- Include Custom Logic
  - User-Defined Peripherals



- Hardware Acceleration
  - Custom Instruction



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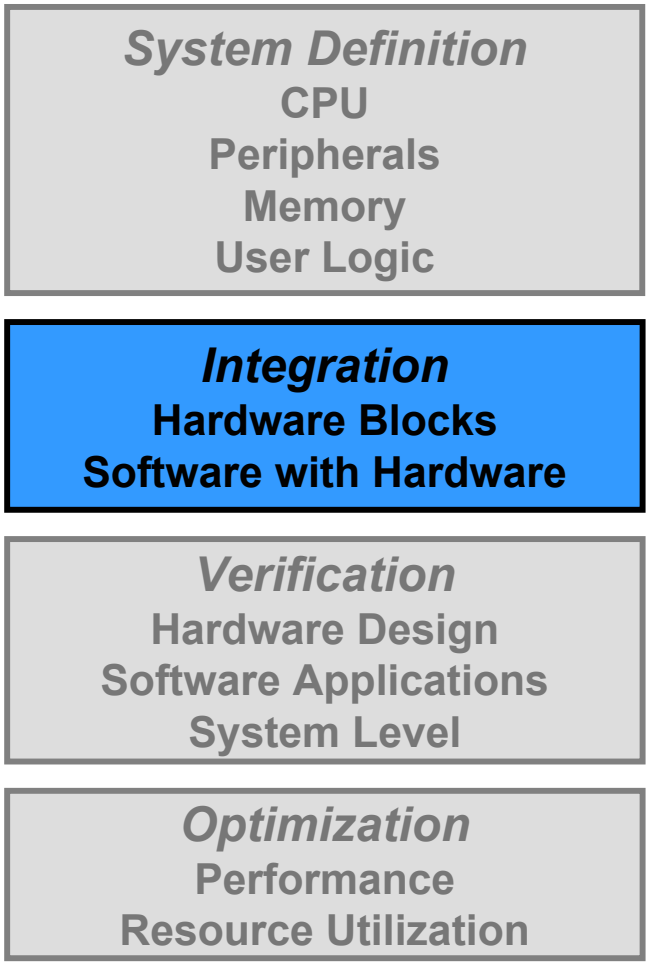
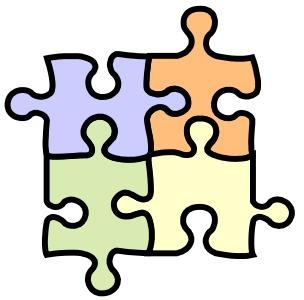


Complex Bus Architecture

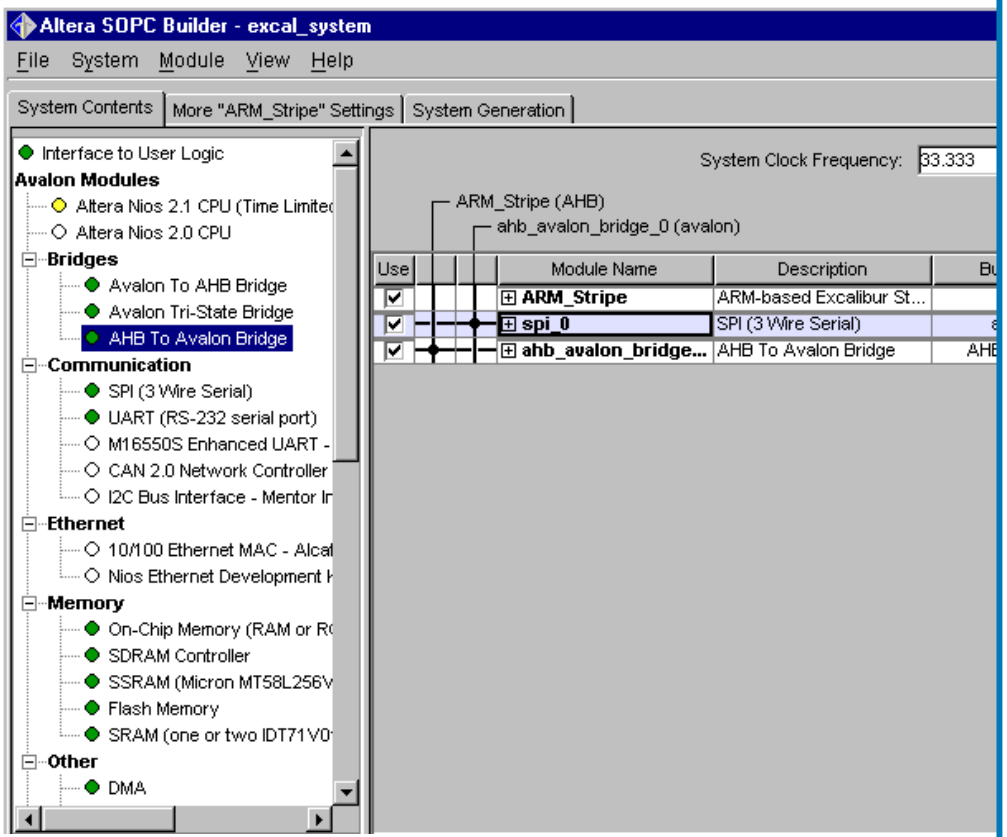
- AHB Master Accessing Non-AHB Peripheral
  - ARM® AHB Master
  - Avalon Slave



- Bridge Required
  - Interfacing between Bus Standard Requires In-depth Knowledge of Both
  - Less than Optimal Bridge Logic Results in Extra Latency
  - Maintain Support for Both Standards Transactions

SOPC Builder Demo

- Bridging Bus Standards



- **Bus Connection Patch Panel**
- **Multi-Master Bus**
  - **Slave-Side Arbitration**
  - **Optimized for Throughput**
- **Bus Bridging**
  - **AMBA™ Advanced High-Performance Bus (AHB)**
  - **Avalon Bus**
  - **Atlantic™ Interface**
  - **PCI**
  - **More to Follow . . .**

Automatic Software Generation

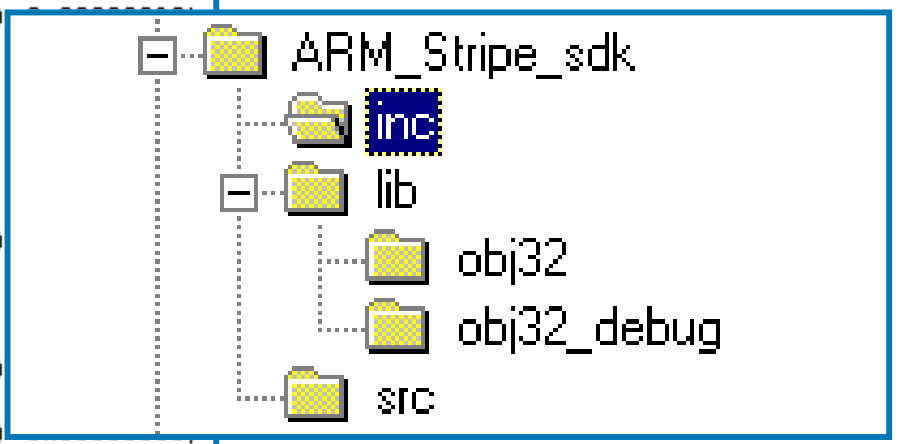
- Software Always Matches Target System

Header file

```
// The Memory Map

#define na_ARM_Stripe              ((void *) 0x00000000)
#define na_ARM_Stripe_base                   0x00000000
#define na_spi_0                   ((void *) 0x80000000)
#define na_spi_0_base                        0x80000000
#define na_spi_0_end               ((void *)
#define na_spi_0_size

#define na_null
#define nasys_vector_table         ((int *)
#define nasys_vector_table_size
#define nasys_vector_table_end     ((int *)
#define nasys_reset_address        ((void *)
#define nasys_clock_freq
#define nasys_clock_freq_1000
#define nasys_debug_core
#define nasys_program_mem          ((void *)
#define nasys_program_mem_size
#define nasys_program_mem_end      ((void *)
#define nasys_data_mem             ((void *) 0x00000000)
#define nasys_data_mem_size                  0x00000000
#define nasys_data_mem_end         ((void *) 0x00000000)
#define nasys_stack_top            ((void *) 0x0003f000)
```



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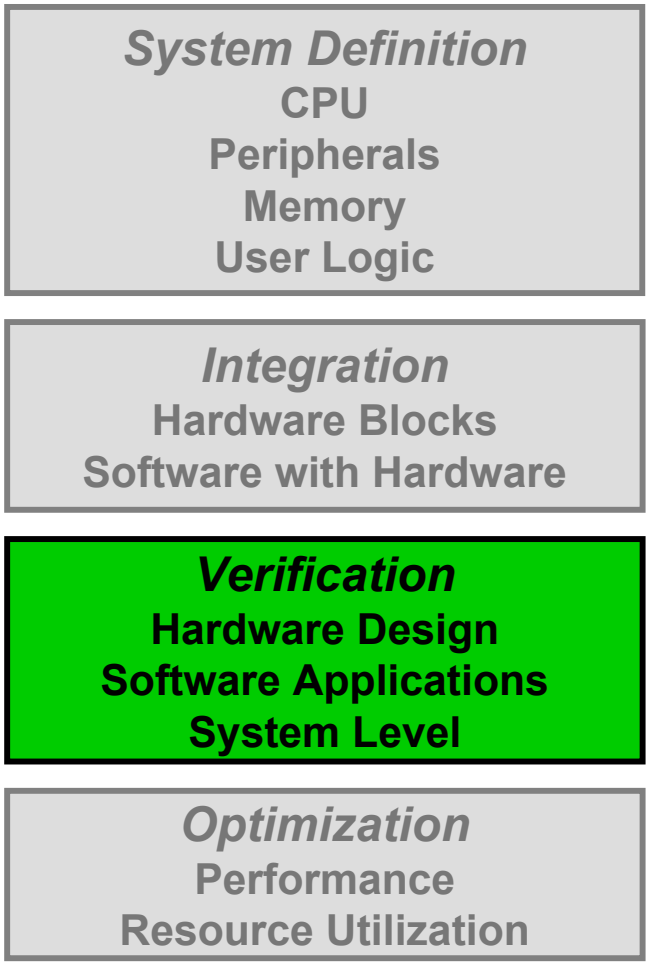
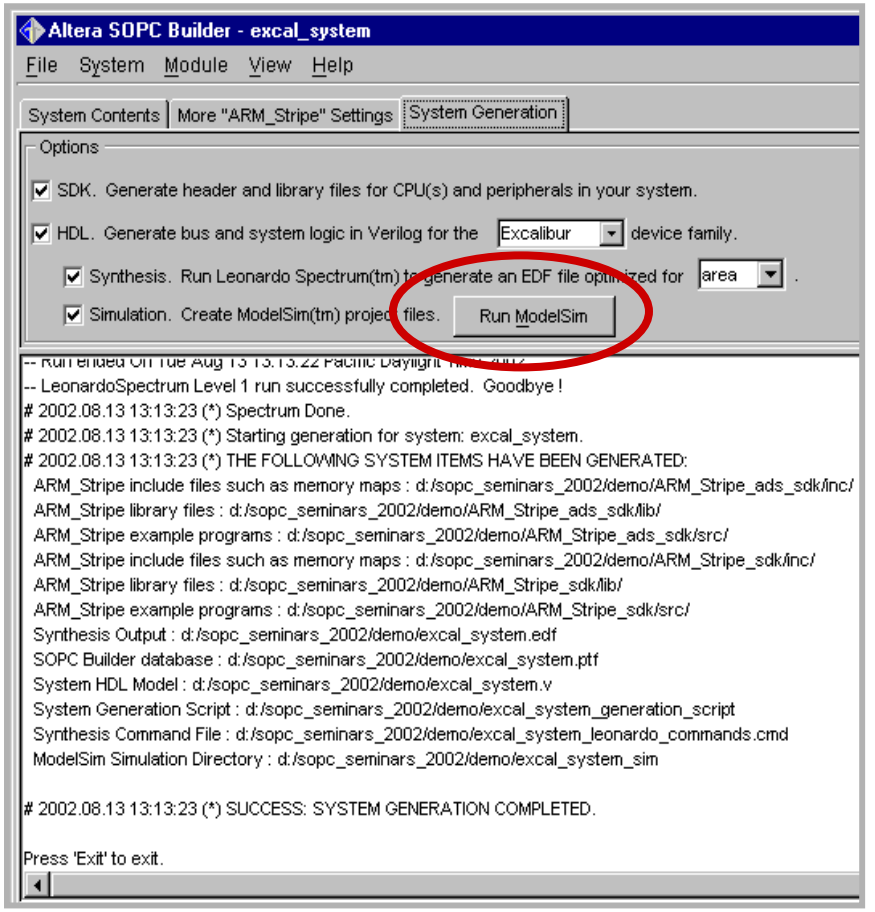


Simulation Test-Bench Creation

- Automatically Creates Complete Testbench
- Initializes System
- Sets up Simulation Environment

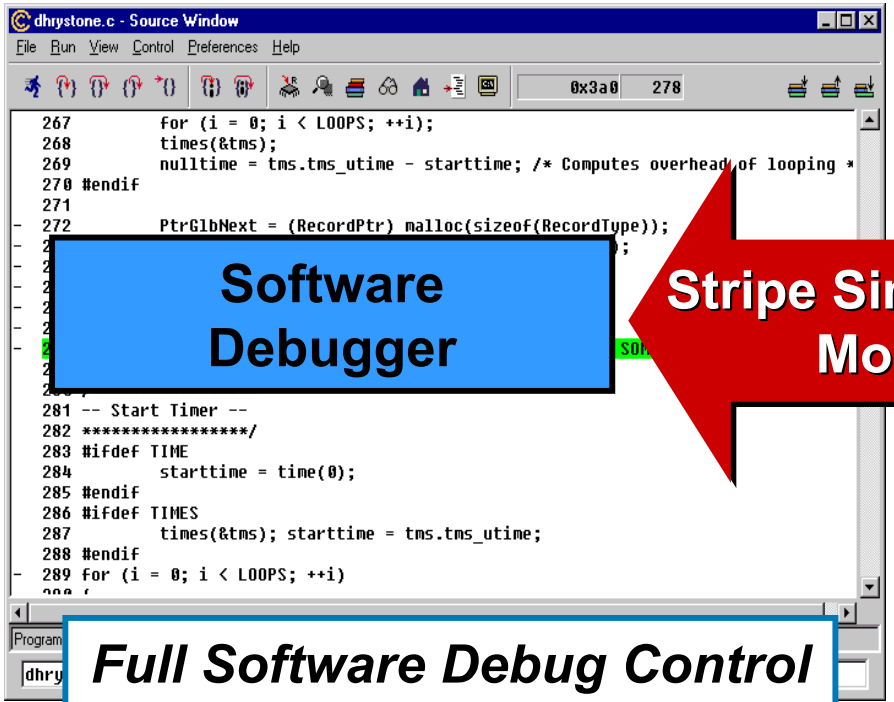


Debugging

- Correlating Software & Hardware Debug Is Challenging
- Software Returns Incorrect Result after Reading Peripheral Register
- Error Could Be in…
  - C Code
  - Memory Map
  - Hardware Address Decoding
  - Hardware Peripheral Logic
  - Read/Write Access Timing for Peripheral

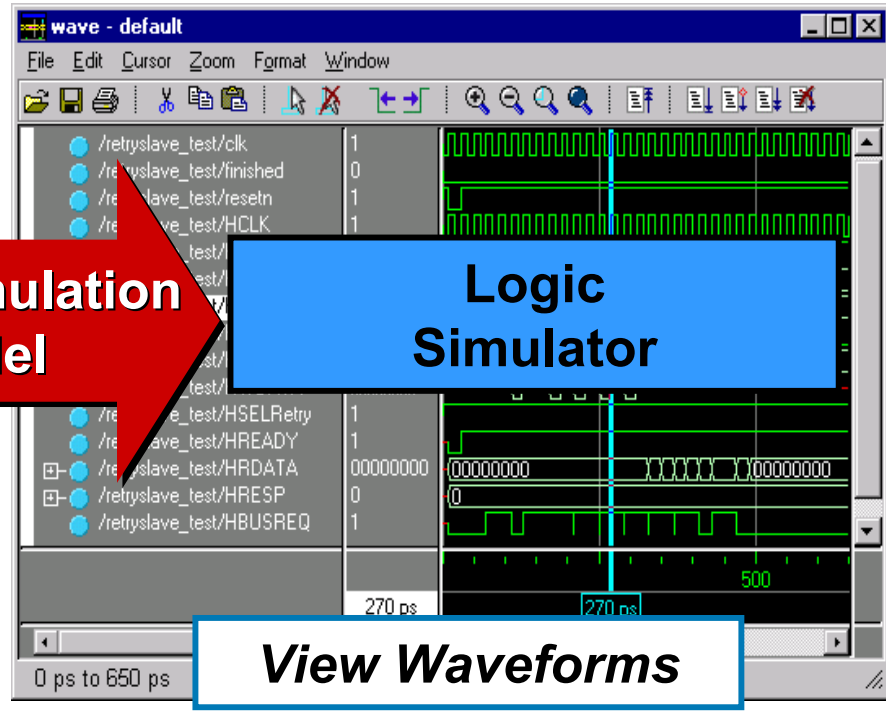
Co-Simulation

- Gain Visibility Into Hardware at Software Breakpoint
- Enables You to Evaluate Required Changes in Hardware or Software



Software Debugger

Stripe Simulation Model



Logic Simulator

Full Software Debug Control
Access to Stripe Registers

View Waveforms

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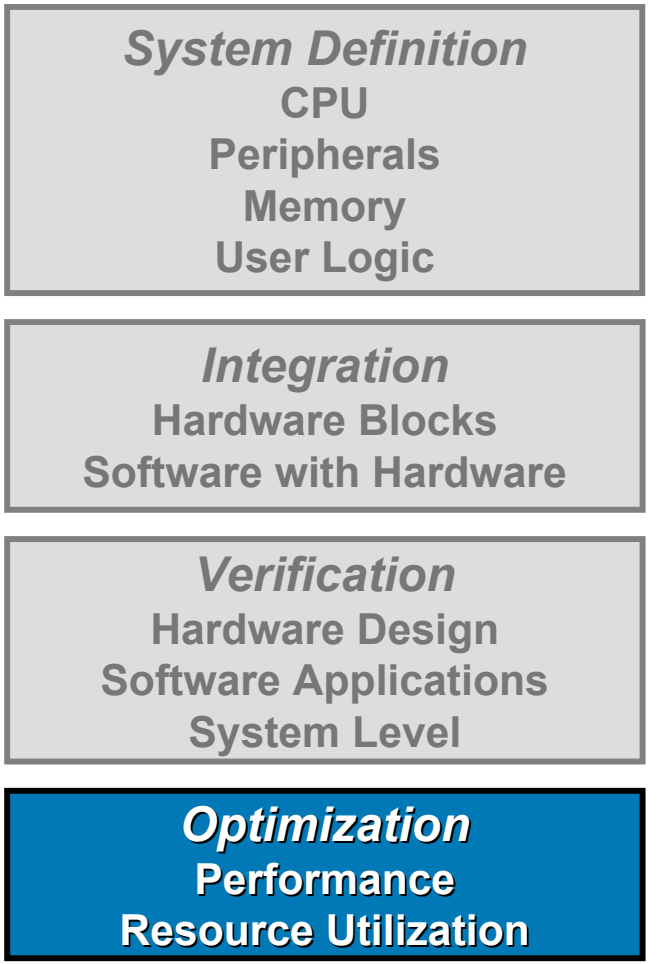
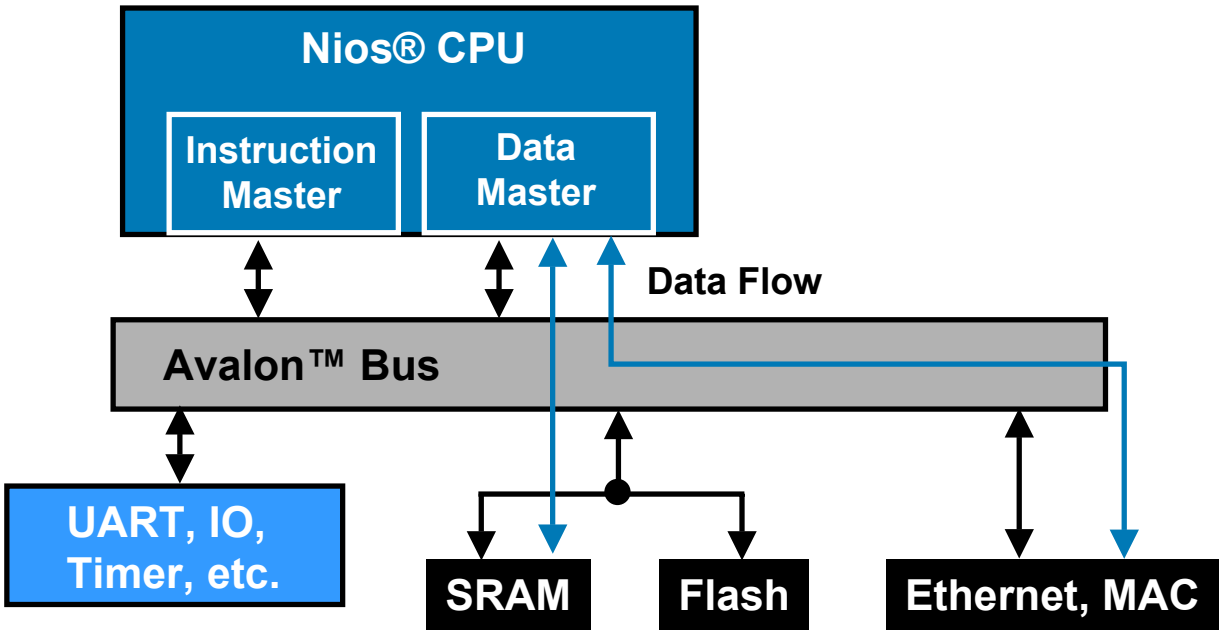


Performance Optimization Example

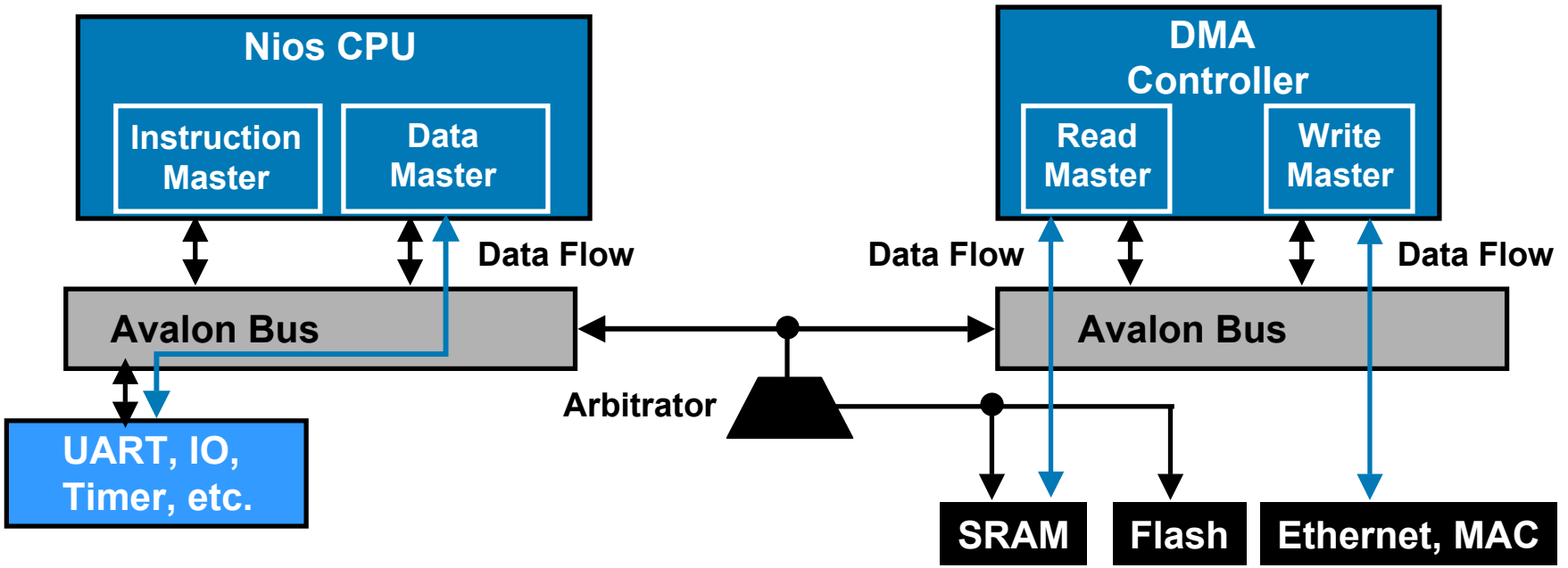
- Web Server Application Using Embedded Processor



File Size (bytes)	Transmission Latency (ms)	Transmission Throughput (Mbps)	HTTP Server Latency (Ms)	HTTP Server Throughput (Mbps)
14,650	38	3.08	57	2.06
37,448	96	3.12	142	2.10
60,036	153	3.14	226	2.12

Optimization 1: DMA Controller

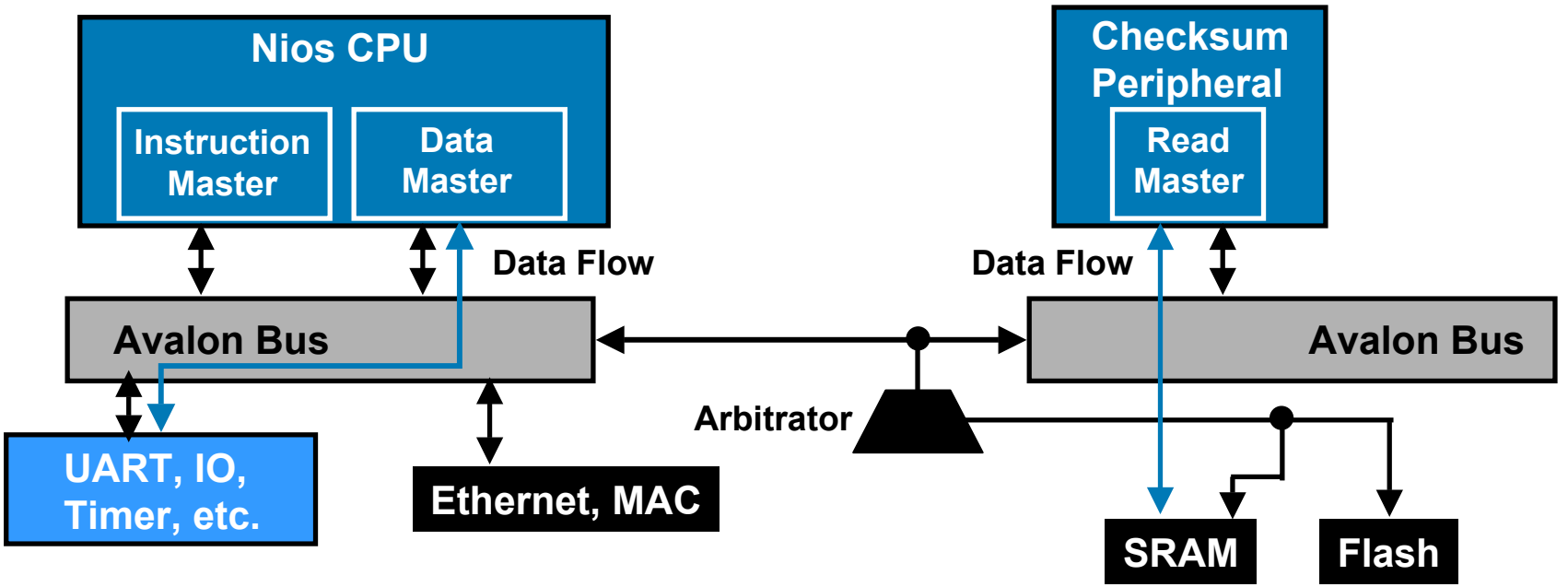
- Adding DMA Controller in FPGA Boosts Throughput 250%



File Size (bytes)	Transmission Latency (ms)	Transmission Throughput (Mbps)	HTTP Server Latency (ms)	HTTP Server Throughput (Mbps)
14,650	18	6.50	24	4.88
37,448	44	6.81	58	5.16
60,036	71	6.76	94	5.10

Optimization 2: Checksum Peripheral

- Moving Checksum Calculation to Hardware Boosts Throughput 25%



File Size (bytes)	Transmission Latency (ms)	Transmission Throughput (Mbps)	HTTP server Latency (ms)	HTTP Server Throughput (Mbps)
14,650	27	4.37	45	2.60
37,448	68	4.40	114	2.62
60,036	109	4.40	181	2.65

Combined Optimization Improvement

- Addition of Both DMA Controller & Checksum Peripheral Increase Server Throughput 280%
- FPGA Logic Element Usage Increased only 65%
- No Board Re-Spin Required

File Size (bytes)	Transmission Latency (ms)	Transmission Throughput (Mbps)	HTTP server Latency (ms)	HTTP Server Throughput (Mbps)
14,650	12	9.76	20	5.86
37,448	31	9.66	49	6.11
60,036	51	9.42	79	6.07

Celoxica C-to-Hardware Tools

- Facilitates Hardware Acceleration in Embedded Processor FPGAs
- Supplies High-level Design Tools that Bridge the Gap between Software & Hardware Design
- ANSI-C Based Handel-C Language Used to Describe Hardware Behavior
- For More Information, Go to www.celoxica.com

Summary

- Programmable Logic Provides
  - Effective Platform for Hardware/Software Co-Design
  - System-Level Integration
  - Flexibility for System Customization
  - Methods for Fast, Effective Verification