Actel® Silicon Explorer II

User's Guide

Windows® Environments

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Table of Contents

Introduction

This manual describes procedures for connecting and using Silicon Explorer II (SE II), debugging, and analyzing devices. For a more detailed description, refer to the online help system included with the software (select the Help command from the Help menu).

Silicon Explorer II enables control of the ActionProbe circuitry, a patented architectural feature built into all of Actel's antifuse devices that allows access to any internal node from selected external pins. SE II integrates two diagnostic tools, the Command module and the Analyze module, into a single diagnostic and logic analysis device that attaches to a PC's standard COM port.

The Command module of the Explore software lists all the observable nets in the FPGA. Select the desired net in the list and click the PRA or PRB button to display the signal on the Analyze module. The Command module also reads back the design's checksum. You can use the design's checksum to verify that you programmed the correct design in the FPGA. The Analyze module is an 18-channel logic analyzer that automatically displays the signals for both probe outputs (and up to 16 additional signals) on the target system. You may sample data asynchronously or synchronously at 100 MHz. Channel 1 and 2 of the logic analyzer connect to the PRA and PRB signals on the FGPA automatically. Silicon Explorer II uses the remaining 16 channels of the logic analyzer to examine other signals on the board.

Actel also offers Silicon Explorer II Lite. SE II Lite enables only the Command module and relies on an external scope or logic analyzer for viewing signals.

System Requirements

The system requirements for Silicon Explorer II and Silicon Explorer II Lite are:

- Designer R1-2000 or later
- Pentium-133 or equivalent
- Microsoft® Windows 95, 98 or NT™ 4.0
- 8 MB RAM (minimum); 16 MB recommended

Connecting to the PC

Silicon Explorer II and Silicon Explorer II Lite connect to a standard serial port using an 8250 or 16550 UART. Establish communication via the 9-Pin D-Sub connector.

Software Settings

Silicon Explorer II sets itself to Demo mode on installation. From the Device menu, select Silicon Explorer II or Silicon Explorer, depending on your version of the software. Choose the desired port (COM1 through COM4) from the Port drop-down list in the Device menu. The software continuously polls the hardware for activity. Setting the port to the Demo mode prevents the application from opening any COM ports on your system. The serial port saves information in the "analyze.ini" file found in your Windows directory. The default data transfer speed is 115,200 baud. At this speed data transfer for the entire buffer is less than 15 seconds.

You can download the latest version of the Explorer software from the Actel website at http://www.actel.com/support/updates or at http://www.actel.com/custsup/updates/siliexp/index.html

Note: Many notebook computers share the external COM port with a built-in infrared (IR) port. You may have to enter your CMOS setup menu to enable the external COM port.

1

Connecting Silicon Explorer II

This section describes the procedures required to connect Silicon Explorer II to your device, powering Silicon Explorer II, SE II connector types, logic analysis, and the Explore software.

Powering Silicon Explorer II

SE II draws power from the external power supply (provided) or by connecting the V_{IO} pin to a power source (such as might exist on a PCB). You must connect V_{IO} to a reference voltage when using the external power supply. Actel recommends using the external power supply when the target system cannot supply enough current to run SE II. See Table 1-1 for a list of possible power configurations.

Table 1-1. Power Configurations for Silicon Explorer II

I/O Power Supply	External SE II Power Supply	VIO
2.5V	Required	2.5V
3.3V	Optional[a]	3.3V
5.0V	Optional[a]	5.0v

a. If your current system is limited, you must use the external power supply and use VIO as the reference voltage. See Table 1-2 for more information about SE II current requirements.

When you apply power, the yellow “heart beat” LED on Silicon Explorer II begins to blink.

Actel designed Silicon Explorer II hardware to withstand abuse normally found in a lab environment. However, long term exposure to out-of-range conditions can cause failure. In particular, long term connection to reverse- or over-voltage power conditions can cause thermal failure.

Current Consumption

Silicon Explorer II is a CMOS device and exhibits very low current consumption when idle. Current consumption rises rapidly to several hundred milliamps during acquisition. If your power supply is unable to supply the necessary current, SE II or your target may reset. Table 1-2 is a guide to typical current consumption based on an acquisition rate at 5V — current will be proportionately higher at 3V.

Table 1-2. Typical Current Consumption

Acquisition Rate	Current@5V
IDLE	75ma
10 MHz	300ma
20 MHz	400ma
50 MHz	500ma
100 MHz	700ma

Connector Types

Silicon Explorer II has a 22-pin (18 channels, a clock, VIO, GND, and clock GND) and a 16-pin connector for controlling the ActionProbe circuitry and reading the design checksum. Silicon Explorer II Lite has only the 16-pin and 26-pin connector (the large 26-pin connector is not used). Table 1-3 is a summary of the connector pins and their functions.

Table 1-3. Connector Types

Connector Type	Mode
22-pin	Logic Analysis
16-pin	ActionProbe Control

Logic Analysis

Note: This section does not apply to Silicon Explorer II Lite.

Actel Silicon Explorer II ships with a replaceable target cable assembly (TCA-8020A) that interfaces Silicon Explorer II with your target system. To connect Silicon Explorer II, align the short red wire on the TCA-8020 with the red dot on the case and fully insert the 2mm header. The contacts on the TCA-8020 accept standard 0.025" round or square test accessories.

Connect any of Silicon Explorer IIs 18-channel leads to the desired target signals using standard test accessories. For synchronous sampling, connect the CLKIN lead to the target clock, which requires a continuous signal. If the clock is greater than 20 MHz, connect the CLK GND (twisted pair) to a ground point near the CLK lead.

Probe Leads

Connect the probe leads by attaching one of two supplied cable assemblies.

One 16-pin cable assembly terminates in individual 0.025 connectors that connect to 0.025 headers or microclips according to the labels on the wires. The other assembly interfaces directly to the target board with a 16-pin header when you install the target according to the pin-out shown in Figure 1-1.

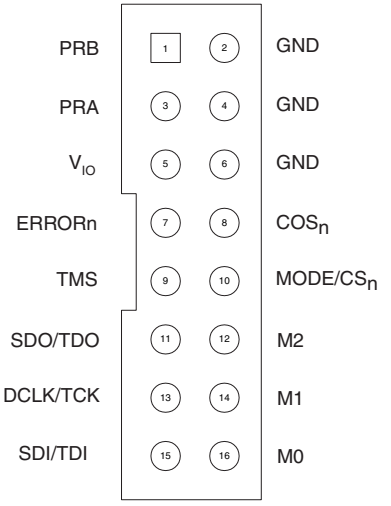


Figure 1-1. Silicon Explorer II Probe Connector Pin-Out

Connect the probe leads according to Table 1-4 below.

Table 1-4. Matching Probe Pins to Device Pins [a]

Probe	Act1, 40MX	ACT2, 42MX, 3200DX	SX/SX-A/eX
Mode	Mode	Mode	Not Used
GND[b]	GND	GND	GND
SDI/TDI	SDI	SDI	TDI
DCLK/TCK	DCLK	DCLK	TCK
SDO/TDO	PRA	SDO	TDO
TMS	Not Used	Not Used	TMS
V_{IO}	V_{CCI}	V_{CCI}	V_{CCI}
PRA	PRA	PRA	PRA
PRB	PRB	PRB	PRB

a. ERRORn, CONn, M2, M1, M0 pins are not required for use with Silicon Explorer II.

b. You may connect any or all GND pins.

Connecting Silicon Explorer II

The diagrams below describe, in detail, how to connect the Silicon Explorer II for the various device families. Figure 1-2 shows how to connect Silicon Explorer II to the ACT1/A40MX devices, Figure 1-3

shows the setup for ACT2/XL/ACT3/DX and A42MX devices, and Figure 1-4 shows the correct setup for SX/SX-A and eX devices.

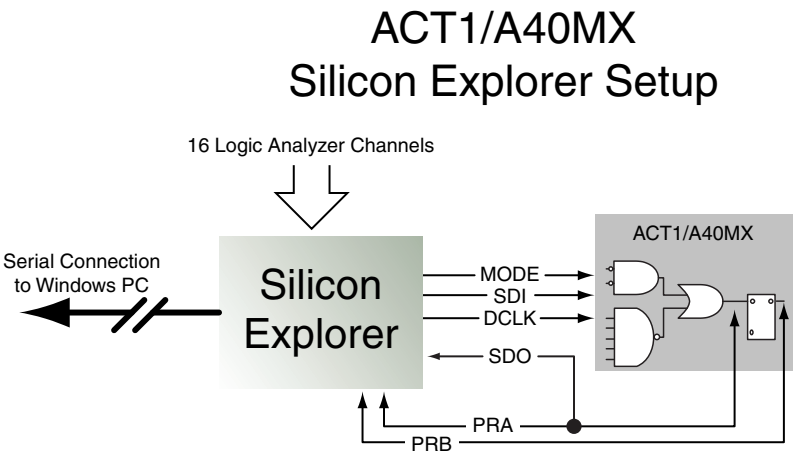


Figure 1-2. ACT1/A40MX Silicon Explorer II Setup

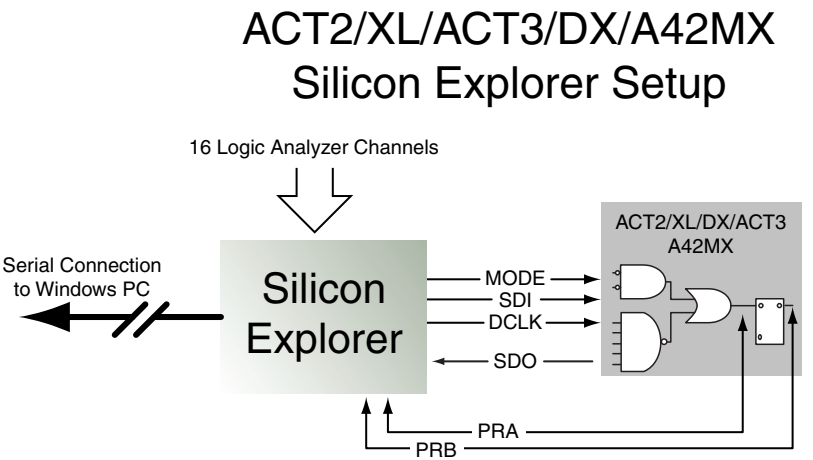


Figure 1-3. ACT2/XL/ACT3/DX/A42MX Silicon Explorer II Setup

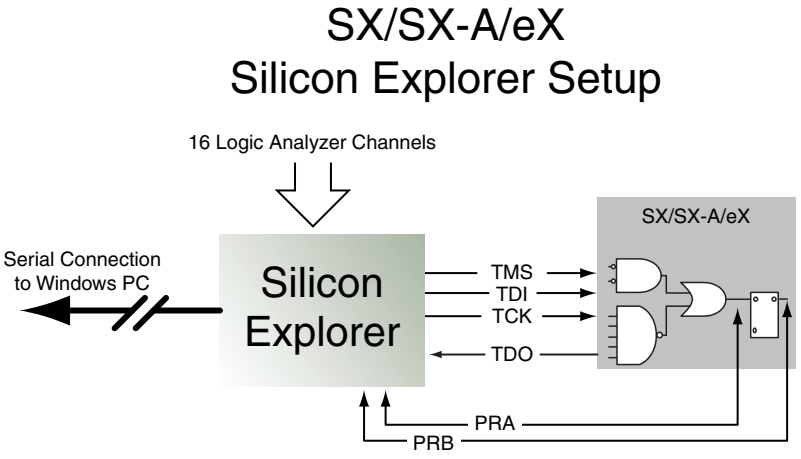


Figure 1-4. SX/SX-A/eX Silicon Explorer II Setup

The probing of an SX-A or eX device may require special setup because it Actel recommends that you use a series 70 ohm termination on all the probe connectors (TDI, TDO, TCK, TMS, PRA, PRB). The 70 ohm series termination is used to prevent data transmission corruption during probing and reading checksum.

2

Silicon Explorer Software

The Explorer software consists of two components, the Command module and the Analyze module. The Command module of the Explore software lists all the observable nets in the FPGA. Use the Command module to verify that you programmed the correct design in the FPGA. The Analyze module is an 18-channel logic analyzer that automatically displays the signals for both probe outputs (and up to 16 additional signals) on the target system.

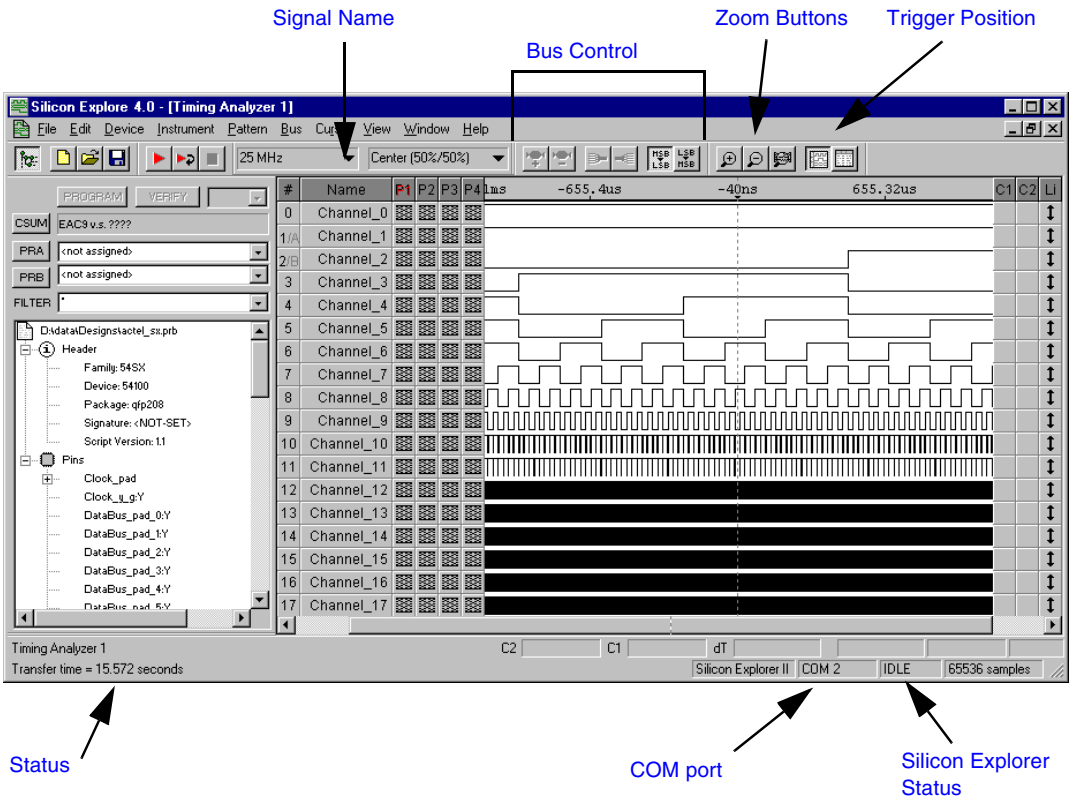


Figure 2-1. Silicon Explore Window

Using the Command Module

The Command module is the interface used to select internal nodes in the Actel FPGA family. The following sections describe exploring with the probe.

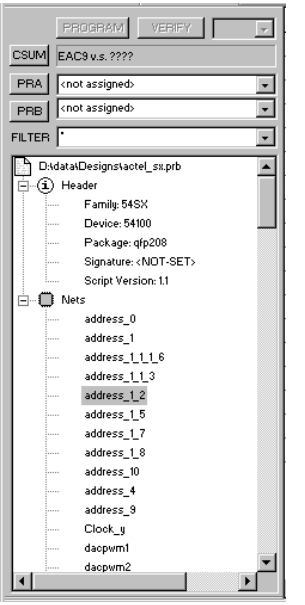


Figure 2-2. Command Module

Explore the FPGA

The following procedures describe how to use the Command module to examine an Actel FPGA.

To open a probe file:

1. **Launch Silicon Explorer.** Select Silicon Explorer from the Designer menu under Programs in the Start menu.
2. **Select a Probe (.prb) file to open.** Select the Open command from the File menu. Choose (*.prb) as the File type and double-click

the desired probe file. You may also open a probe file in Silicon Explorer by double-clicking the "Open Actel Probe File" icon.

Explore uses a .prb file exported from Designer during analysis. The exported file contains device information, net names, and node location information. After the .prb file opens, verify the information displayed in the tree structure in the Analyze window.

To export a probe file from Designer:

1. **Launch Designer.**
2. **Open your design file.**
3. **Open the Export dialog box.** Select Export from the File menu to view the Export dialog box (Figure 2-3).

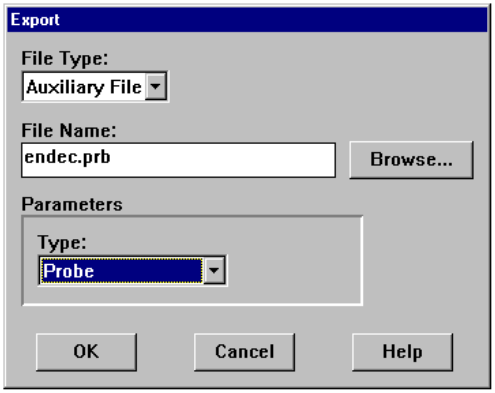


Figure 2-3. Designer File Export Dialog Box

4. **Select Auxiliary File from the File Type pull-down menu.**
5. **Select Probe from the Type pull-down menu.**
6. **Select OK to continue.**

To verify the checksum:

First, ensure that that the SDO/TDO is connected. Then click the Checksum button. Once you open a Probe file and make a device connection, read the checksum of the target device and compare it to

the checksum in the Probe file by double-clicking the Checksum button. Table 2-1 lists and explains the error messages.

Table 2-1. Checksum Error Messages

Error Message	Explanation
Checksum: 383A vs. ????	Checksum is not readable because the probe is disconnected or not powered.
Checksum: 383A vs. 0000	The checksum does not match the file. **or** The SDO/TDO probe-side pin is not properly connected to the device. Please see Table 1-4 on page 6 for the proper connection.

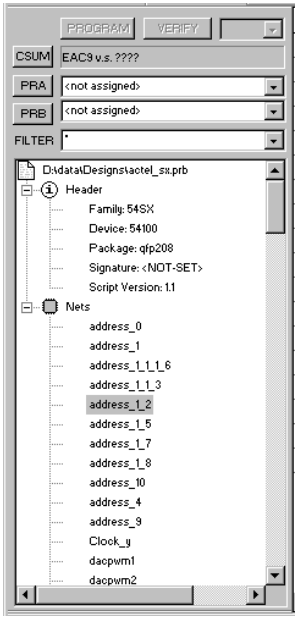
To probe a node:

1. **Select the desired signal from the tree by clicking the net name (see Figure 2-1).** You can use the filter box to search nets quickly. Use multiple wildcard characters ("*") to restrict your search.
2. **Click the PRA or PRB button.** Silicon Explorer II routes the selected node to the probe pin and switches the corresponding analyzer input to the probe connector. The Analyze module displays the net name.

You can modify the tree information to reflect the design's internal net names or pin names by right-clicking the Nets icon and selecting either

"Show Nets" or "Show Pins". See Figure 2-4 for examples of the two types of displays.

"Show Nets" Display



"Show Pins" Display

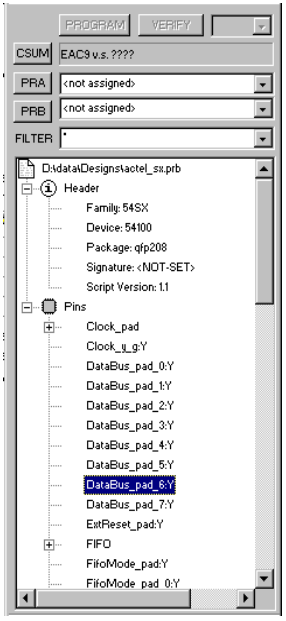


Figure 2-4. Command Module Display Styles

If you cannot find a net, it is possible that the net was optimized by Designer. Refer to "Troubleshooting" on page 27 for more information about the limitations in probing Actel devices using Silicon Explorer.

Using the Analyze Module

Note: This section does not apply to Silicon Explorer II Lite, since it does not contain the Analyze module.

Open Silicon Explorer II and check the status in the lower right corner of the display. If you have properly selected the COM port and powered up Silicon Explorer II, then the status is IDLE. The Analyze

module captures 64K samples of each channel and uploads them to the host over the serial port.

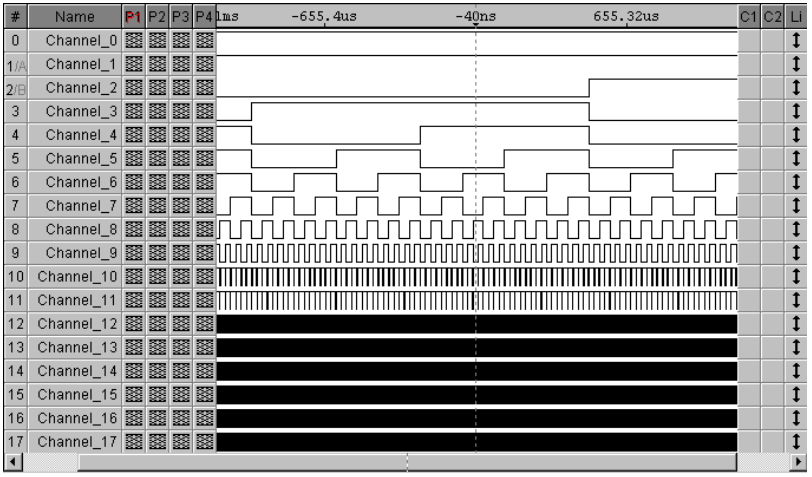


Figure 2-5. Analyze Module

Set acquisition parameters from the tool bar or the pull-down menus. See Table 2-2 for a summary of the parameters.

Table 2-2. Acquisition Parameters

Acquisition Speed	10 Khz to 100 MHz asynchronous or synchronous to 100 MHz
Trigger Position	25% to 75% 50% to 50% 75% to 25%
Trigger Pattern	Click on individual signals in the T column to specify don't care, low, high, rising, falling or either edge. The trigger pattern is the logical AND of the 18 patterns.

Once you set the acquisition parameters, click the Run button (red triangle) to begin acquisition. The analyzer begins capturing data. After you acquire the initial 64K samples, sampling continues until Silicon

Explorer II recognizes the trigger pattern or you press the stop button (black square). During the capture period, the status window displays "PRE" for the pretrigger state (although you may not see it if the trigger pattern matches quickly).

Next, Silicon Explorer II enters the "POST" state and samples data after the trigger pattern (or stop button) until it fulfills the posttrigger requirement. Then, it uploads the data to the host (READ State with progress indicator). The entire upload process takes less than 15 seconds, although you may zoom in and view data immediately because the buffer uploads as a background task.

View Data

Panning and zooming are available in the scroll bars, tool bar, or keyboard control. In addition, dragging a box in the display area zooms the window. Table 2-3 lists keyboard equivalents.

Table 2-3. Keyboard Equivalents

Key	Function
Up Arrow	Zoom In 2X
Down Arrow	Zoom Out 2X
Left Arrow	Scroll Earlier (Data moves Right)
Right Arrow	Scroll Later (Data moves Left)
Page Up	Jump One Screen Earlier
Page Down	Jump One Screen Later
Home	Jump to Trigger

Place cursors by clicking in the display area. Silicon Explorer II displays the time below the channel labels and data values in the C1 and C2 columns. The L or "Live" Column indicates the current state of the 18 channels when the analyzer is in "IDLE."

The Timing Instrument offers many convenient features for viewing, saving, and printing data. More detailed information is available from the online help system (select the Help command from the Help menu).

A

Debugging SX/SX-A/eX Devices Using Silicon Explorer II

SX, SX-A, and eX devices may require additional attention when debugging. You must control probing on SX and SX-A devices through the IEEE 1149.1 pins. You may configure the IEEE 1149.1 pins as dedicated (JTAG only) or flexible (JTAG or I/O). This section assists you with these and other considerations when debugging SX, SX-A, or eX devices.

Probe Circuit Control Pins

The Silicon Explorer II tool uses the IEEE 1149.1 ports (TDI, TCK, TMS and TDO) to select the desired nets for debugging. The user assigns the selected internal nets to the PRA/PRB pins for observation. Figure A-6 illustrates the connection between Silicon Explorer II and the SX/SX-A/eX FPGA required to perform in-circuit debugging.

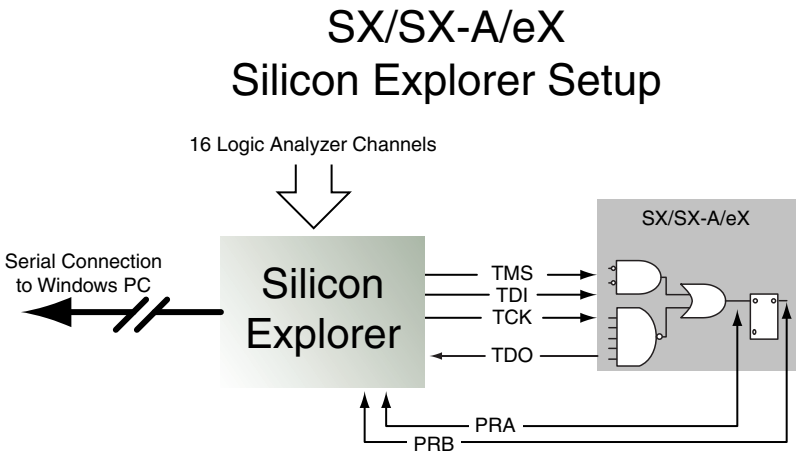


Figure A-6. Probe Setup

Diagnostic Pin Consideration

To place the IEEE 1149.1 (JTAG) and probe pins (TDI, TCK, TMS, TDO, PRA and PRB) in the desired mode, select the appropriate check boxes in the "Device Variations" dialog window (as shown in Figure A-7). This dialog window is accessible through the Design Setup Wizard under the Option menu in Designer.

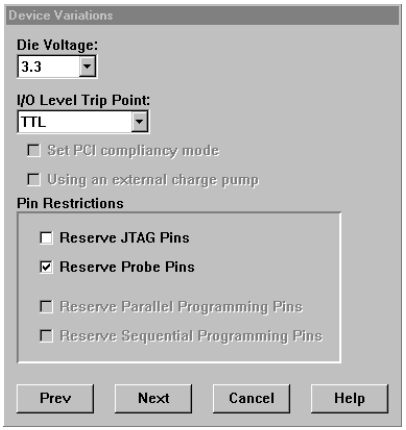


Figure A-7. Diagnostic Pins Configuration

To Access the Device Variations Dialog Box in Designer:

1. **Launch Designer.**
2. **Open your Design.**
3. **Select Device Setup under the Options Menu.** The Device Selections dialog box appears.
4. **Click Next.** The Device Variations Dialog Box appears.

Dedicated JTAG Mode

When you select the "Reserve JTAG Pin" box, you place the FPGA in **Dedicated JTAG mode**, which configures TDI, TCK, and TDO pins for JTAG boundary scan or in-circuit debug with Silicon Explorer II. Also, you enable an internal pull-up resistor on both the TMS and TDI pins (Figure A-8). In addition, by checking the "Reserve JTAG Pin" box,

TDI, TCK and TDO are not available for pin assignment in the Pin Editor.

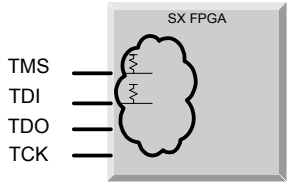


Figure A-8. Dedicated JTAG Mode

You do not need to specify an internal pull-up resistor; SE II automatically configures TMS and TDI with internal pull-up resistors.

Flexible JTAG Mode

When you do not select the "Reserve JTAG Pin" box, you place the FPGA in **Flexible JTAG mode**, where TDI, TCK and TDO pins may function as user I/Os or JTAG pins. When you select Flexible JTAG mode, you disable the internal pull-up resistors on the TMS and TDI pins. Note that you require an external 10K Ohm pull-up resistor on the TMS pin in this mode (Figure A-9).

Silicon Explorer II transforms TDI, TCK and TDO pins from user I/Os into JTAG diagnostic pins when a rising edge at TCK is detected while TMS is at logical low. The JTAG pins revert to user I/Os when the JTAG state machine is in the Test-Logic reset state.

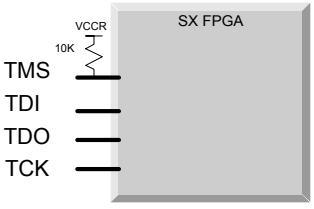


Figure A-9. Flexible JTAG Mode. Note 10K Ohm Pull-up Resistor

Table 1 enumerates all the possible configuration of the diagnostic pins.

Table 1. Diagnostic Pin Configuration

Dedicated JTAG Mode	Flexible JTAG Mode
• TCK, TDI, and TDO are dedicated diagnostic pins.	• Use TCK, TDI and TDO as I/Os. • You need the 10K pull-up resistor on the TMS Pin.

Probe Pins

When you select the "Reserve Probe Pin" box, you direct the layout tool to reserve the PRA and PRB pins as diagnostic pins. This option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/O's to achieve successful layout, then the tool will use these pins as user I/Os. If you assign user I/Os to the PRA and PRB pins and select the "Reserve Probe Pin" option, the Layout tool will override the "Reserve Probe Pin" option.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit.

Location of the SDO Pin

Package	SDO Pin #
14100	
BGA313	AE23
PGA257	R17
QFP208	103
QFP256	126
RDQFP208	103
1415	
LCC68	52
LCC84	52
PGA100	L9
QFP100	77
VQFP100	49
1425	
LCC84	52
PGA132	52
PGA133	M11
QFP100	77
QFP132	63
QFP160	79
VQFP100	49
1440	
LCC84	52
PGA175	N12
PGA176	52
QFP100	52
QFP160	79
QFP172	52
QFP176	87
QFP208	52
VQFP100	49
1460	
BGA225	N13
LCC84	52
PGA207	P15
QFP160	79
QFP176	87
QFP196	99
QFP208	103

Package	SDO Pin #
32100	
LCC84	52
QFP160	82
QFP176	87
QFP208	103
QFP84	42
32140	
BGA240	AC3
LCC84	52
QFP160	82
QFP176	87
QFP208	103
QFP256	67
32200	
CQFP208	103
QFP208	103
QFP240	123
QFP256	67
RDQFP20	106
RQFP208	106
32300	
QFP240	123
QFP256	67
RDQFP20	106
3265	
LCC84	52
QFP100	52
QFP160	82
QFP176	87

Package	SDO Pin #
42MX09	
LCC84	52
QFP100	52
QFP160	82
QFP176	87
VQFP100	50
42MX16	
LCC84	52
QFP100	52
QFP160	82
QFP176	87
QFP208	103
VQFP100	50
42MX24	
LCC84	52
QFP160	82
QFP176	87
QFP208	103
42MX36	
BGA272	V18
CQFP208	103
CQFP256	67
QFP208	103
QFP240	123
1225/1225XL	
LCC84	52
PGA100	J9
QFP100	52
VQFP100	50
1240/1240XL	
LCC84	52
PGA132	N12
QFP100	52
QFP144	71
QFP176	87
1280/1280XL	
LCC84	52
PGA176	P13
QFP160	82
QFP172	85
QFP176	87
QFP208	103

Package	SDO Pin #
54SX08	
QFP208	103
VQFP100	49
TQFP144	71
TQFP176	87
54SX16	
QFP208	103
VQ100	49
TQ176	87
CQFP208	103
CQFP256	126
54SX16P	
QFP208	103
VQ100	49
TQ144	71
TQ176	87
54SX32	
QFP208	103
VQ100	49
TQ144	71
TQ176	87
BGA313	AE23
BGA329	AA20
54SX08A	
PQFP208	103
TQ100	49
TQ144	71
54SX16A	
PQ208	103
TQ100	49
TQ144	71
54SX32A	
PQFP208	103
TQ144	71
BGA329	AA320
54SX72A	
PQFP208	103
BGA484	AB20

Figure B-1. SDO Pin Location Table

C

Termination of the VPP and Mode Pin for ACT1 Devices in a Radiation Environment

There is a concern about the use of Actel RH1020 or RH1280 Field Programmable Gate Arrays (FPGA) in a space-flight, radiation-environment with the MODE and/or VPP pins left unterminated. The effects of a floating VPP pin are difficult to assess. Testing indicates that the VPP pin must be properly terminated for reliable operation of the device.

MODE Pin

The MODE pin is used to control both the state of the device (e.g., normal, programming, debug, outputs disabled, various test modes, etc.) and the operation with regular logic levels. The device can be put into various modes; when the MODE pin is in the logic one state, commands can be shifted into the internal registers via DCLK (Data Clock) and SDI (Serial Data In), and through proper sequencing. When the MODE pin is in the logic zero state, all of the mode registers and control path flip-flops are directly held in the inactive state, guaranteeing that the device is in normal operating mode. Note that there is no guarantee as to the states of these “configuration” registers at power-up.

The effects of a floating MODE pin are difficult to predict because almost anything can happen. For example, one state that the device might go into is to support board level test. In this mode, all of the device outputs are tristated. Other examples of possible modes include programming mode and various device test modes. Incorrect configuration can result in functional failures and/or high currents which may either damage or pose a serious reliability hazard to the hardware. The effects for damage to the device and the board must be assessed on a specific basis.

Testing shows that when the MODE pin is tied high, it is easy to “latch-up” the device with heavy ions. The devices repeatedly draw excessive amounts of current. The probability of having a problem with an unterminated MODE pin is quite high.

Actel recommends that you terminate the MODE pin to a GND with a hard jumper in parallel with a 10k W resistor. The hard jumper protects against resistor failure. During the prototype and debug stage you can remove the hard jumper and utilize the Silicon Explorer probing capability. Verify the termination of the MODE pin for each Actel device on the flight board with an ohm meter. Programming the security/probe fuse does not eliminate the need to terminate the mode pin.

VPP Pin

The VPP pin is the input supply pin used for device programming (the Radiation-Hardened FPGAs' data sheet refers to pin 22 on the RH1020 and pin 107 on the RH1280 as VCC). Actel recommends that you do not leave VPP floating, since it may bounce around and a high voltage might put the device in programming mode. For operating in a radiation environment, there is a concern that unterminated leads can charge up. In various radiation cases this effect has been observed.

Under normal operating conditions (MODE low and VPP high), the VPP signal is used to bias transistors in the peripheral control circuitry of the FPGA and does not directly access the user-defined logic modules or fuses in the array core. When the device is in programming mode (MODE pin high), the VPP signal can reach every module in the array core. If the MODE pin is not properly terminated, there is a risk that the device could go into programming mode and lose all functionality. If MODE is tied low and VPP is not properly terminated, then there is a risk of damage to the peripheral control circuitry of the gate array.

The VPP pin is designed to receive voltages exceeding VCC. Under normal operating conditions, the VPP signal is used to bias a high voltage FET along with the drain of that FET. In flight, the FET would break down at lower bias voltages. Various tests and analyses showed that in the radiation environment, a single ion was capable of rupturing an antifuse at 5 VDC, which corresponds to an electric field strength of approximately 6 MV/cm. Factors for rupture include electric field strength, oxide quality and uniformity, and any parasitic junctions that may be biased.

Internally, a diode exists between the VCC and VPP signal. Under normal operating conditions (VPP tied high), this diode cannot be forward-biased and the device draws normal operating current as outlined in the Actel FPGA Data Book. If this diode becomes forward biased (a potential risk if VPP floats and gets driven low), the device draws excessive current. Also, we have found that the VPP pin is the most sensitive pin to ESD on the RH1020 and RH1280.

Actel recommends that you connect the VPP pin be directly to the VCC. Additionally, verify with an ohm meter that the VPP pins on all flight devices are properly terminated.

Actel does not guarantee the long-term reliability of devices that were not always in a legal operating configuration. No credible analysis has been performed that would guarantee reliable operation of parts that were not always in a legal operating configuration.

D

Troubleshooting

The following is a list of frequently asked questions for Silicon Explorer II. For more information, visit the Actel online support website at http://www.actel.com/guru. This chapter is divided into four sections:

- Errors and troubleshooting
- General information
- Software setup
- Hardware setup

Errors and Troubleshooting

Q: I've connected Silicon Explorer II and the window display reads N/C. Why?

A: Look on the top of the Silicon Explorer II for the flashing yellow "heartbeat." If it isn't flashing make sure you have properly connected an adequate power supply.

Q: It's flashing but still N/C. Why?

A: There are a number of things that prevent you from establishing communication. The following are the most common:

- Wrong COM port. Try all four COM ports, even if you are sure that your mouse is on COM 1.
- No power to Silicon Explorer II (see above).
- Desktop Systems External connector not connected to the COM port internally.
- Laptop systems external COM connector disabled (IR Port Override?). Use your PC's CMOS setup program to enable the COM port.
- COM port IRQ reassigned for DOS program, control panel not updated.
- Multiple mouse drivers in system.ini.

- Third-party serial port “enhancers” do not conform to windows API.

Q: I’ve got the IDLE message, but when I click on Run, the Silicon Explorer II window flashes an error message and returns to IDLE. Why?

A: If the target power is incapable of supplying the necessary current, then Silicon Explorer II resets and returns to IDLE. Many current-limiting supplies will trip when set too close to the operating current.

Q: The Analyze module acquires data and then indicates errors on read-back. Why?

A: The Analyze module bursts data back in blocks at high speeds, with built-in retry for a bad block (it uses both checksum and byte count). Some third-party serial programs block all interrupts, forcing the analyzer into a retry loop.

Some laptops power down the UART and drop a few characters. Try disabling “Power Saving” in the CMOS setup menu.

Q: When the Explore window is open, my other Windows programs run slowly. Why?

A: If the Explore window is open but not connected or powered up, then the system is constantly timing out looking for a response. Either close the SE II window or change the COM port to DEMO.

Q: I get a message “Device Timed out” when I try to assign a particular signal to the Probe pins. Why?

A: This message gives us an indication that the power is not sufficient for the Silicon Explorer and as a solution you would have to add a separate power source for the Silicon Explorer. Refer to “Powering Silicon Explorer II” on page 3 for more information.

Q: I have assigned an internal signal to PRA and PRB but the PRA and PRB light is not blinking on the Probe Pilot. Is this normal?

A: The PRA and the PRB light on the Probe Pilot are just an indication of the logic level of that assigned internal signal. If the assigned internal net is at permanent logic 0, the light on the Probe Pilot for the corresponding probe will not glow.

Q: My cable does not have the TMS and the SDO pins. Why?

A: Your cable will not have the TMS and the SDO pin cables if it was bought before the SX probing capability was introduced. To order a new cable (Si-Ex-Ribbons), contact Actel customer service at Customer.Service@actel.com.

Q: Is the Silicon Explorer displaying an incorrect signal?

A: Make sure that the signal is sampled at a sufficiently high frequency. The sampling rate should be at least twice the frequency of the fastest changing signal. The maximum frequency at which the signal can be sampled is 100 MHz which limits the frequency of the device to 50MHz. If a higher sampling frequency is required than the PRA and the PRB pins can be connected to a logic analyzer to view the signals.

Q: Why can't I find the net I wish to probe?

A: Silicon Explorer lists only the signals which are actually present on the device. There is a possibility that the net which you wish to probe has been optimized in Designer. Please check the list of the nets combined in the combiner file (*.cob) which is exported from Designer File>Export>Auxillary File with file type *.cob

Q: What are the limitations in probing Actel devices using Silicon Explorer?

A: Probing limitations are described in Table D-1. Note that -- indicates that the feature is unavailable, and * indicates that the feature only applies to devices that have Qclock.

Table D-1. Probing Limitations

Family	Probe Capable			
	Input	Clock	Hclock	Qclock
ACT1[a]/40MX	Y	Y	--	--
ACT2/XL/42MX	Y	Y	--	--
ACT3	Y	Y	Y	--
DX/42MX	Y	Y	--	Y*[b]
SX/SX-A/eX	N	Y	N	N*[c]

a. For old ACT1 devices (specifically A10xx, A10xxA, some A10xxB, all TI material, and Military ACT1) the probed signal is inverted. We do not have a specific break point in the lot numbers for A10xxB devices, however if you provide the lot number to us, we will try to determine if that lot has inverted probe signals. Of course the best way to know for sure is to probe the output of an input buffer and compare the Silicon Explorer reading with the applied value.

b. QCLKINT signal is inverted and may be swapped with an adjacent quadrant as described in the following Guru document:
http://www.actel.com/apps/guru/oct98/hw1668.html

c. QClock probe ability for SX-A is currently disabled but may become available in the future.

General Information

Q: Does Silicon Explorer support ProASIC programming and debugging?

A: No. As of today Silicon Explorer does not support either ProASIC programming or debugging.

Q: What are the accessories available for the Silicon Explorer?

A: Silicon Explorer Accessories:

SI-EX-RIBBONS:Ribbon cable assembly for FPGA probe connection (for both Silicon Explorer and Silicon Explorer lite)

SI-EX-TCA: Flying lead cable assembly

Q: Can we use Silicon Explorer to debug devices which have their security fuses programmed?

A: As a part of the Actel FPGAs security feature the Silicon Explorer cannot be used on devices which have their security fuse programmed.

Q: Can I use the probe pins as regular I/Os?

A: All of the probe pins can be used as user I/O except for the MODE and TMS pins. Once the device enters probe mode, The I/O's switch to the probe functionality. We highly recommend that you do not use these pins as inputs, since your device will not accept the inputs during probe mode.

Q: What are the differences between Silicon Explorer I and Silicon Explorer II?

A: The main difference between Silicon Explorer I and Silicon Explorer II is that the Silicon Explorer II logic-analysis system was enhanced to support an external power supply, which permits internal probing of 5.0V, 3.3V, and 2.5V FPGAs. Other features include four-levels of triggering, decompression on download to speed up response time and system acquisition rates up to 100MHz.

Software Setup

Q: How do I set up triggering?

A: You have an option of setting trigger either EARLY that displays the values in the ratio of (25% 75%), where the first % represents the % of data sampled before the trigger point and the later % represent % sampled after the trigger point. The other options available are CENTER(50% 50%) and LATE(75% 25%). You can select the trigger position from Instrument -> Trigger Position and then selecting the required Trigger position.

Q: What is the recommended sampling rate?

A: For an accurate reading, the sampling rate for a particular signal should be at least twice the rate at which the signal is changing (According to the Nyquist theorem). For example, a clock operating at 25MHz should be sampled at least 50MHz frequency. Sampling at higher frequencies however causes the Silicon Explorer to consume more power.

Q: What is the best way to find nets?

A: The best way to find the nets in the Silicon Explorer is to use the Filter option available in the software. You can search for the net you require by using the *partial_name* in the filter, which would return all the signals having that partial_name of the net. If you are using an HDL flow, it may be difficult to recognize the net names you need to observe. We recommend that you use a synthesis tool that can generate a gate-level schematic of your synthesized netlist so that during probing, you can easily trace through the schematic and obtain the net names from it.

Hardware Setup

Q: How do I probe an SX-A device?

A: The probing of an SXA device requires special setup because it requires a 70 ohm termination on all the probe connectors (TDI, TDO, TCK, TMS, PRA, PRB). The 70 ohm series termination is used to prevent data transmission corruption during probing.

Q: How do I tie the TRST pin during the probing using Silicon Explorer?

A: TRST is an active low input. During JTAG mode and Silicon Explorer debugging mode, JTAG state machine's reset must not be active, otherwise probe circuitry is disabled. Below is the recommendation for TRST pin in JTAG and Silicon Explorer:

RTSX Rev0 - No TRST pin

RTSX Rev1 - You must tie TRST pin high when doing JTAG and Silicon Explorer

RTSX Rev2 - You can leave the TRST pin floating (or drive it high - it must not be driven low) when running JTAG or Silicon Explorer if “Reserve JTAG TRST” was selected in Designer.

SXA - You can leave the TRST pin floating when running JTAG or Silicon Explorer

Q: What are the different options that I have to connect a device to Silicon Explorer Probe Pilot?

A: You can connect the Silicon Explorer to the device by either implementing a probe connector on the board for use with the ribbon connector or by connecting the device to the Probe-Pilot using the flying lead connector. If you choose the second alternative, you can either use posts on your board, or the clips provided with the Si Explorer to connect directly to the probe pins Please refer to question 16 for information about the probe connector dimensions.

Q: Where can I get the mechanical dimensions for the Silicon Explorer's Probe connector?

A: Please refer to the following guru document for detailed information about the connector. http://www.actel.com/GURU_docs/feb00/ns853.html.

Q: Where can I find the pin layout of the Silicon Explorer?

A: The pin layout for the Silicon Explorer is found on the back of the Silicon Explorer case. There is a notch on one side of the pin connector that determines the position of Pin 1.

Q: How is the checksum of the device read?

A: The checksum of most devices is read through the SDO pin. For information about the location of SDO pins in all Actel Devices please refer to “Location of the SDO Pin” on page 21.

ACT1 and the 40MX pins do not have an SDO pin. In order to read the checksum from ACT1/40MX devices the PRA on the device must be connected to the SDO pin of the Silicon Explorer.

Q: What are the power requirements for Silicon Explorer II?

A: Silicon Explorer II must be connected to a power supply of 5V for 5V tolerant devices, 3.3V for 3.3V tolerant devices, and 2.5V for 2.5V tolerant devices.

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