ProASIC Macro Library Guide

June 1999

Actel

Actel Corporation, Sunnyvale, CA 94086

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Trademarks

This Library Guide replaces all earlier editions of similar product series.

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1 Combinational Cells

The Pro ASIC A500K combinational cells implement all basic logic functions and have the following features:

- Inversion available on all inputs.
- Optimized for synthesis applications.

Naming Conventions for Combinational Cells

Names for combinational cells are composed of two parts:

- A name identifying the logic function (AND2, NOR3, XOR2, BFR, etc.).
- A 2- or 3-character code describing the pin inversions such as TFF. Capital T (true) indicates not inverted and capital F (false) indicates inverted. When no inputs are inverted, the inversion code is omitted.

Note: Not all combinations of inverted inputs are available. We have limited the number to avoid redundancy (e.g. AND2FF is logical equal to NOR2).

For Example:

AND2FT - The cell is a 2-input AND gate. The pin inversion code FT indicates that the A input pin is inverted, and the B input pin is not inverted.

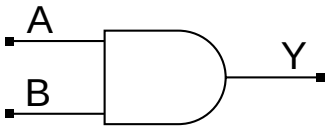
AOI21FTF - The cell is a 2-input AND gate into a 2-input NOR gate. Pin A and C are inverted, pin B is not.

Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- X - indicates either logic level one or zero (don't care).

AND2



Function

2 Input AND

Truth Table

A	B	Y
1	1	1
0	X	0
X	0	0

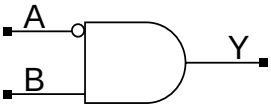
Input

A, B

Output

Y

AND2FT



Function

2 Input AND with Active Low A Input

Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

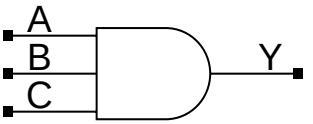
Input

A, B

Output

Y

AND3



Function

3 Input AND

Truth Table

A	B	C	Y
1	1	1	1
X	X	0	0
X	0	X	0
0	X	X	0

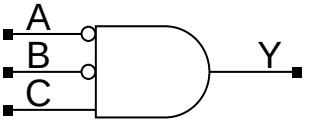
Input

A, B, C

Output

Y

AND3FFT



Function

3 Input AND with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

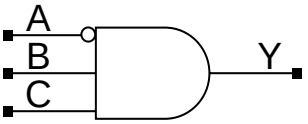
Input

A, B, C

Output

Y

AND3FTT



Function

3 Input AND with Active Low A Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

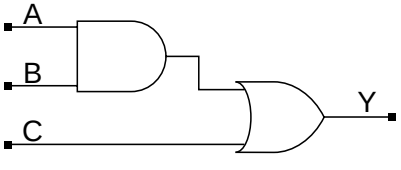
Input

A, B, C

Output

Y

A021



Function

3 Input AND-OR

Truth Table

A	B	C	Y
0	X	0	0
X	0	0	0
X	X	1	1
1	1	X	1

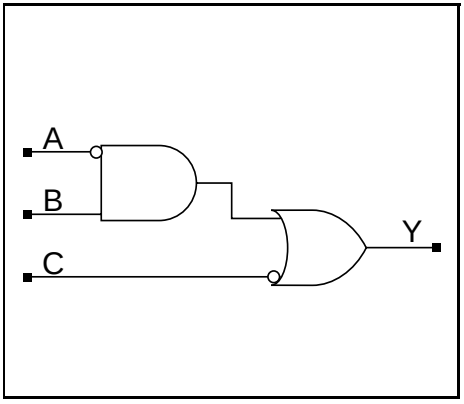
Input

A, B, C

Output

Y

A021FTF



Function

3 Input AND-OR with Active Low A and C Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

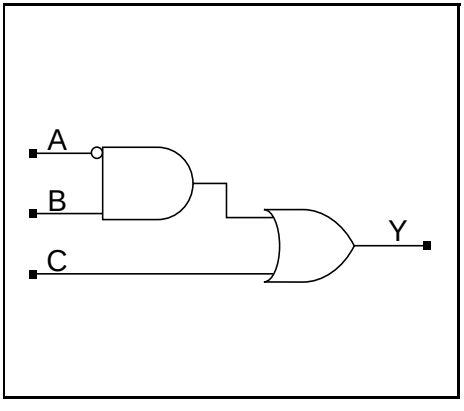
Input

A, B, C

Output

Y

A021FTT



Function

3 Input AND-OR with Active Low A Input

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

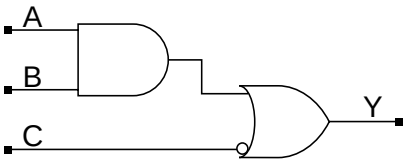
Input

A, B, C

Output

Y

A021TTF



Function

3 Input AND-OR with Active Low C Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

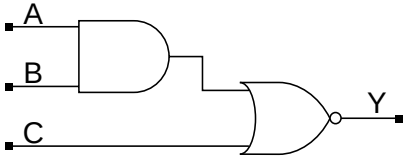
Input

A, B, C

Output

Y

A0I21



Function

3 Input AND-OR-INVERT

Truth Table

A	B	C	Y
0	X	0	1
X	0	0	1
X	X	1	0
1	1	X	0

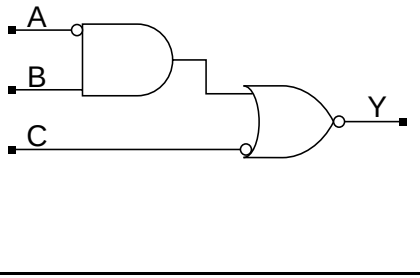
Input

A, B, C

Output

Y

AOI21FTF



Function

3 Input AND-OR-INVERT with Active Low A and C Inputs

Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	1	X	0
1	X	1	1

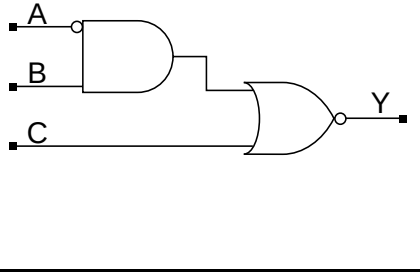
Input

A, B, C

Output

Y

AOI21FTT



Function

3 Input AND-OR-INVERT with Active Low A Input

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

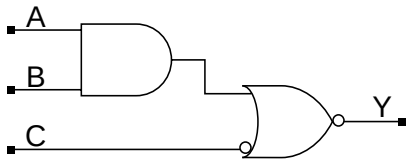
Input

A, B, C

Output

Y

AOI21TTF



Function

3 Input AND-OR-INVERT with Active Low C Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

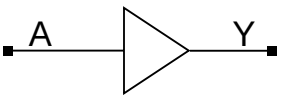
Input

A, B, C

Output

Y

BFR



Function

Buffer

Truth Table

A	Y
0	0
1	1

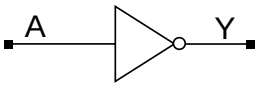
Input

A

Output

Y

BUBBLE



Function

Inverter (Only for internal embedded memory)

Truth Table

A	Y
0	1
1	0

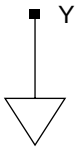
Input

A

Output

Y

GND



Function

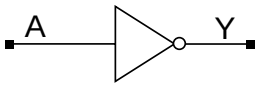
Ground

Input

Output

Y

INV



Function

Inverter

Truth Table

A	Y
0	1
1	0

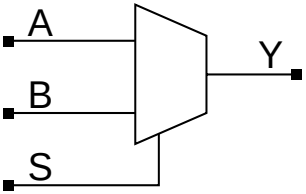
Input

A

Output

Y

MUX2H



Function

2 to 1 Multiplexer

Truth Table

S	Y
0	A
1	B

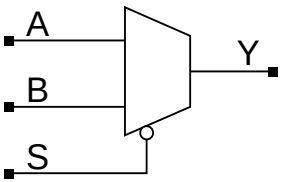
Input

A, B, S

Output

Y

MUX2L



Function

2 to 1 Multiplexer with Active Low Select

Truth Table

S	Y
0	B
1	A

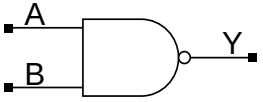
Input

A, B, S

Output

Y

NAND2



Function

2 Input NAND

Truth Table

A	B	Y
1	1	0
0	X	1
X	0	1

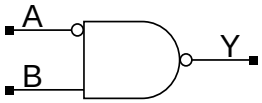
Input

A, B

Output

Y

NAND2FT



Function

2 Input NAND with Active Low A Input

Truth Table

A	B	Y
1	X	1
0	1	0
X	0	1

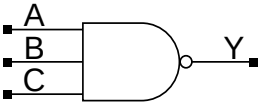
Input

A, B

Output

Y

NAND3



Function

3 Input NAND

Truth Table

A	B	C	Y
1	1	1	0
0	X	X	1
X	X	0	1
X	0	X	1

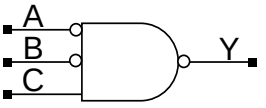
Input

A, B, C

Output

Y

NAND3FFT



Function

3 Input NAND with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

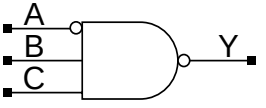
Input

A, B, C

Output

Y

NAND3FTT



Function

3 Input NAND with Active Low A Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

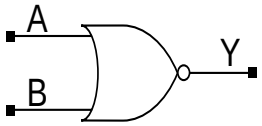
Input

A, B, C

Output

Y

NOR2



Function

2 Input NOR

Truth Table

A	B	Y
0	0	1
1	X	0
X	1	0

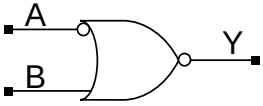
Input

A, B

Output

Y

NOR2FT



Function

2 Input NOR with Active Low A Input

Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

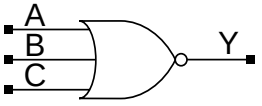
Input

A, B

Output

Y

NOR3



Function

3 Input NOR

Truth Table

A	B	C	Y
0	0	0	1
1	X	X	0
X	X	1	0
X	1	X	0

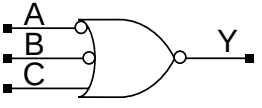
Input

A, B, C

Output

Y

NOR3FFT



Function

3 Input NOR with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

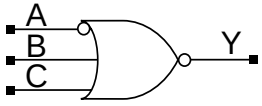
Input

A, B, C

Output

Y

NOR3FTT



Function

3 Input NOR with Active Low A Input

Truth Table

A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

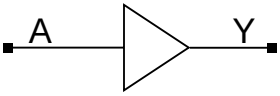
Input

A, B, C

Output

Y

NUBBLE



Function

Buffer (Only for internal embedded memory)

Truth Table

A	Y
0	0
1	1

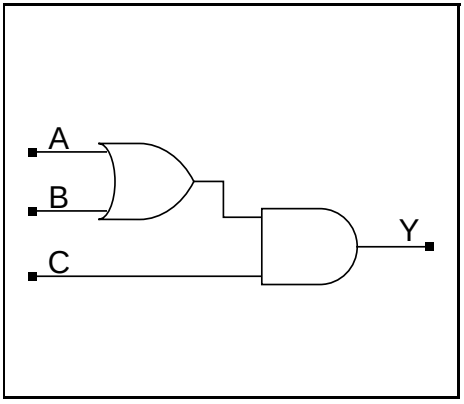
Input

A

Output

Y

OA21



Function

3 Input OR-AND

Truth Table

A	B	C	Y
1	X	1	1
X	1	1	1
X	X	0	0
0	0	X	0

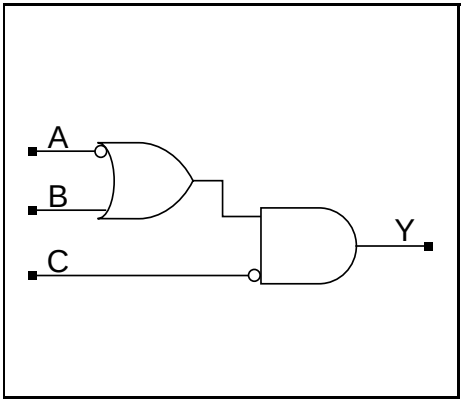
Input

A, B, C

Output

Y

OA21FTF



Function

3 Input OR-AND with Active Low A and C Inputs

Truth Table

A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

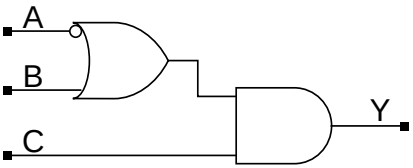
Input

A, B, C

Output

Y

OA21FTT



Function

3 Input OR-AND with Active Low A Input

Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

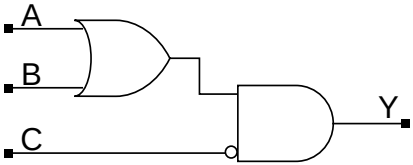
Input

A, B, C

Output

Y

OA21TTF



Function

3 Input OR-AND with Active Low C Input

Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

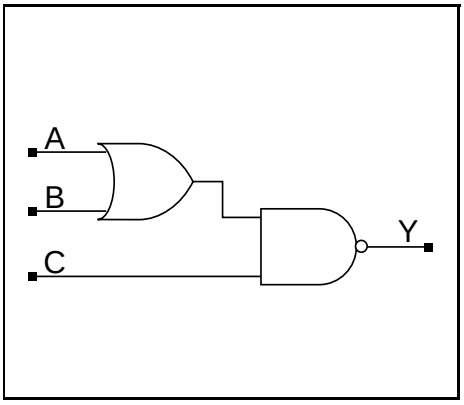
Input

A, B, C

Output

Y

OAI21



Function

3 Input OR-NAND

Truth Table

A	B	C	Y
1	X	1	0
X	1	1	0
X	X	0	1
0	0	X	1

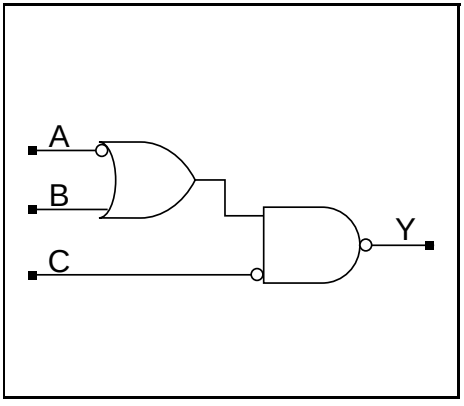
Input

A, B, C

Output

Y

OAI21FTF



Function

3 Input OR-NAND with Active Low A and C Inputs

Truth Table

A	B	C	Y
0	X	0	0
X	X	1	1
1	0	X	1
X	1	0	0

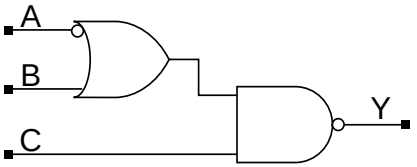
Input

A, B, C

Output

Y

OAI21FTT



Function

3 Input OR-NAND with Active Low A Input

Truth Table

A	B	C	Y
X	X	0	1
0	X	1	0
1	0	X	1
X	1	1	0

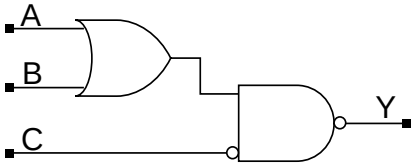
Input

A, B, C

Output

Y

OAI21TTF



Function

3 Input OR-NAND with Active Low C Input

Truth Table

A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

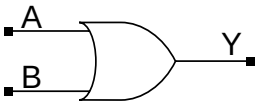
Input

A, B, C

Output

Y

OR2



Function

2 Input OR

Truth Table

A	B	Y
1	X	1
X	1	1
0	0	0

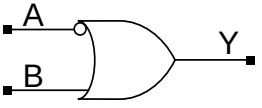
Input

A, B

Output

Y

OR2FT



Function

2 Input OR with Active Low A Input

Truth Table

A	B	Y
0	X	1
1	0	0
X	1	1

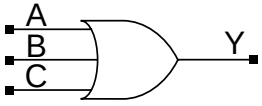
Input

A, B

Output

Y

OR3



Function

3 Input OR

Truth Table

A	B	C	Y
1	X	X	1
X	1	X	1
X	X	1	1
0	0	0	0

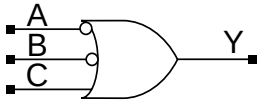
Input

A, B, C

Output

Y

OR3FFT



Function

3 Input OR with Active Low A and B Inputs

Truth Table

A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

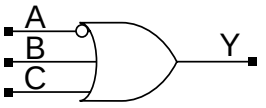
Input

A, B, C

Output

Y

OR3FTT



Function

3 Input OR with Active Low A Input

Truth Table

A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

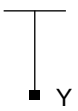
Input

A, B, C

Output

Y

PWR



Function

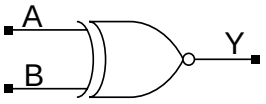
Power

Input

Output

Y

XNOR2



Function

2 Input Exclusive NOR

Truth Table

A	B	Y
0	0	1
1	1	1
1	0	0
0	1	0

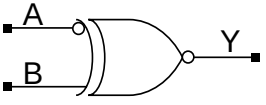
Input

A, B

Output

Y

XNOR2FT



Function

2 Input Exclusive NOR with Active Low A Input

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

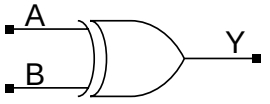
Input

A, B

Output

Y

XOR2



Function

2 Input Exclusive OR

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

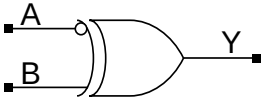
Input

A, B

Output

Y

XOR2FT



Function

2 Input Exclusive OR with Active Low A Input

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Input

A, B

Output

Y

2

Storage Cells

The A500K storage cells implement transparent latch and D-type flip-flop functions and have the following features:

- Inversion available on Enable pin on all latches.
- Optimized for synthesis flows.
- Asynchronous CLR and SET pins.

Naming Conventions for Flip-Flops

Names for the flip-flop cells are composed of four parts:

- A base name identifying the cell as a D-type flip-flop (DFF).
- An optional 1-character code describing the clock pin. L indicates negative edge triggered. No code indicates positive edge triggered.
- Asynchronous input type and polarity: an optional 1-character code designating the control pins as follows:

  B = Active high, **b**oth set and clear
  C = Active high **c**lear
  S = Active high **s**et

  When omitted, the cell has neither SET nor CLEAR input.
- An optional 1-character code describing the output. I indicates output is inverted. No code indicates output is not inverted.

For Example:

DFFC - The cell is a positive edge triggered D-type flip-flop with active high CLEAR.

DFFLB - The cell is a negative edge triggered D-type flip-flop with active high SET and CLEAR.

Naming Conventions for Latches

Names for the latch cells are composed of four parts:

- A name identifying the logic function as a latch (LD).
- An optional 1-character code describing the Enable pin. L indicates active low. No code indicates active high.

- Asynchronous input type: an optional 1-character code designating the control pins as follows:

  B = Active high, **b**oth set and clear
  C = Active high **c**lear
  S = Active high **s**et

  When the latch has neither SET nor CLEAR pins, this code is omitted.

- An optional 1-character code describing the output polarity. I indicates output is inverted. No code indicates output is not inverted.

For Example:

LDL - The cell is a transparent latch with active low enable and neither SET nor CLEAR pins.

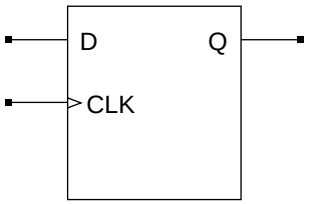
LDLSI - The cell is a transparent latch with active low enable, active high SET pin and inverted output pin named QBAR.

Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- ↑ - indicates positive (rising) edge.
- ↓ - indicates negative (falling) edge.
- D - indicates input port.
- !D - indicates inverted input port.
- Q - indicates output port.
- QBAR - indicates inverted output port.
- X - indicates either logic level one or zero (don't care).

DFF



Function

Positive Edge Triggered D-Type Flip-Flop

Truth Table

CLK	Q_{n+1}
↑	D

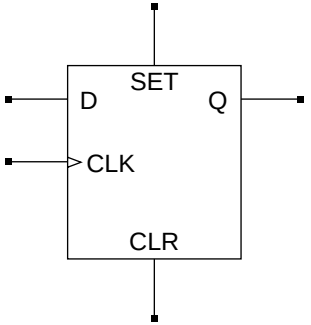
Input

D, CLK

Output

Q

DFFB



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Clear

Truth Table

CLK	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
↑	0	0	D

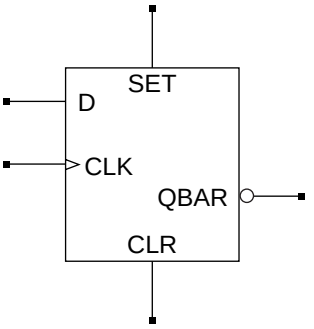
Input

CLR, SET, CLK, D

Output

Q

DFFBI



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Clear and Active Low Output

Truth Table

CLK	SET	CLR	$QBAR_{n+1}$
X	1	0	1
X	X	1	0
↑	0	0	!D

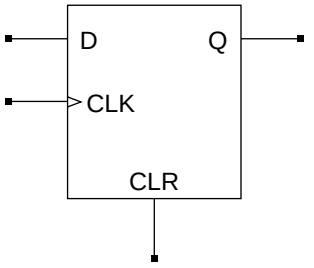
Input

CLR, SET, CLK, D

Output

QBAR

DFFC



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Clear

Truth Table

CLK	CLR	Q_{n+1}
X	1	0
↑	0	D

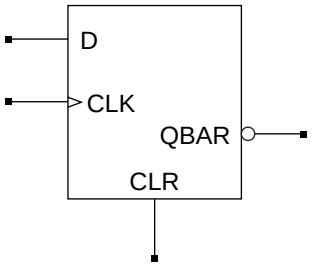
Input

CLR, CLK, D

Output

Q

DFFCI



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Clear and Active Low Output

Truth Table

CLK	CLR	$QBAR_{n+1}$
X	1	1
↑	0	!D

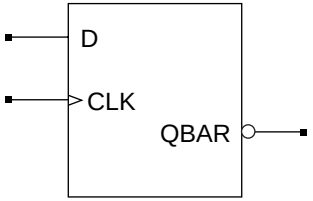
Input

CLR, CLK, D

Output

QBAR

DFFI



Function

Positive Edge Triggered D-Type Flip-Flop with Active Low Output

Truth Table

CLK	$QBAR_{n+1}$
↑	!D

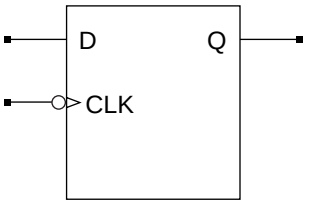
Input

CLK, D

Output

QBAR

DFFL



Function

Negative Edge Triggered D-Type Flip-Flop

Truth Table

CLK	Q_{n+1}
↓	D

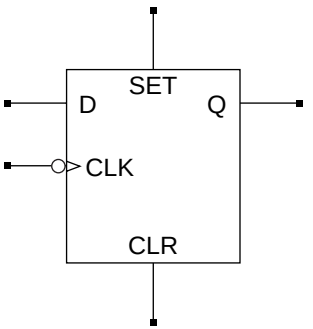
Input

CLK, D

Output

Q

DFFLB



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Clear

Truth Table

CLK	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
↓	0	0	D

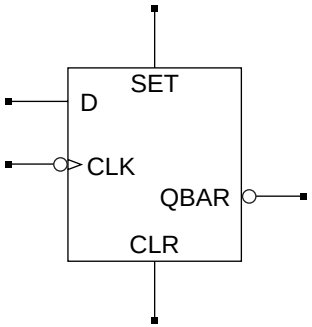
Input

CLR, SET, CLK, D

Output

Q

DFFLBI



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Clear and Active Low Output

Truth Table

CLK	SET	CLR	$QBAR_{n+1}$
X	1	0	0
X	X	1	1
↓	0	0	!D

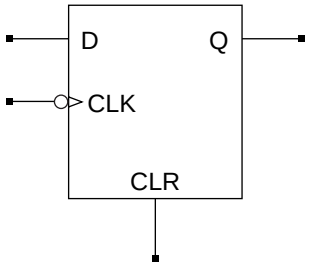
Input

CLR, SET, CLK, D

Output

QBAR

DFFLC



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Clear

Truth Table

CLK	CLR	Q_{n+1}
X	1	0
↓	0	D

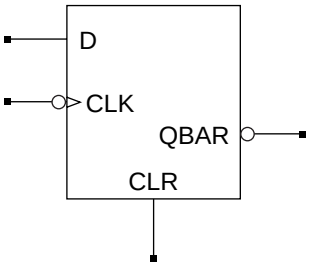
Input

CLR, CLK, D

Output

Q

DFFLCI



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Clear and Active Low Output

Truth Table

CLK	CLR	$QBAR_{n+1}$
X	1	1
↓	0	!D

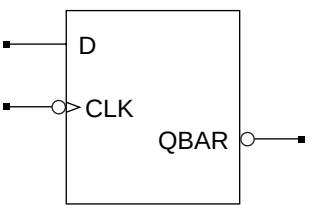
Input

CLR, CLK, D

Output

QBAR

DFFLI



Function

Negative Edge Triggered D-Type Flip-Flop with Active Low Output

Truth Table

CLK	$QBAR_{n+1}$
↓	!D

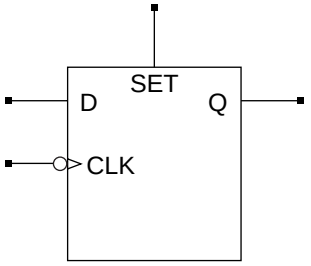
Input

CLK, D

Output

QBAR

DFFLS



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set

Truth Table

CLK	SET	Q_{n+1}
X	1	1
↓	0	D

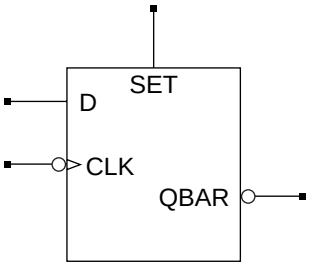
Input

SET, CLK, D

Output

Q

DFFLSI



Function

Negative Edge Triggered D-Type Flip-Flop with Active High Set and Active Low Output

Truth Table

CLK	SET	$QBAR_{n+1}$
X	1	0
↓	0	!D

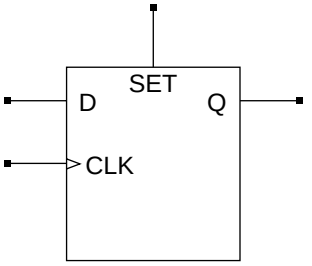
Input

SET, CLK, D

Output

QBAR

DFFS



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Set

Truth Table

CLK	SET	Q_{n+1}
X	1	1
↑	0	D

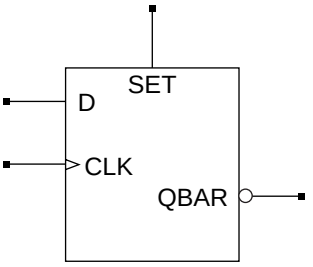
Input

SET, CLK, D

Output

Q

DFFSI



Function

Positive Edge Triggered D-Type Flip-Flop with Active High Set and Active Low Output

Truth Table

CLK	SET	$QBAR_{n+1}$
X	1	0
↑	0	!D

Input

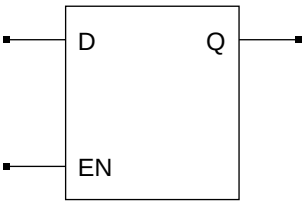
SET, CLK, D

Output

QBAR

Latches

LD



Function

Active High Latch

Truth Table

EN	Q_{n+1}
0	Q
1	D

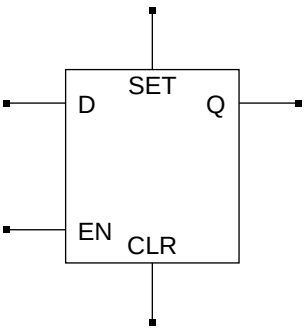
Input

EN, D

Output

Q

LDB



Function

Active High Latch with Active High Set and Clear

Truth Table

EN	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
1	0	0	D
0	0	0	Q

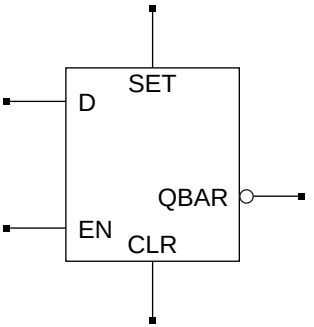
Input

CLR, SET, EN, D

Output

Q

LDBI



Function

Active High Latch with Active High Set and Clear and Active Low Output

Truth Table

EN	SET	CLR	$QBAR_{n+1}$
X	1	0	0
X	X	1	1
1	0	0	!D
0	0	0	QBAR

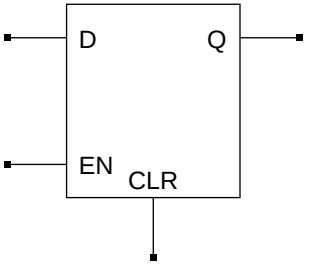
Input

CLR, SET, EN, D

Output

QBAR

LDC



Function

Active High Latch with Active High Clear

Truth Table

EN	CLR	Q_{n+1}
X	1	0
1	0	D
0	0	Q

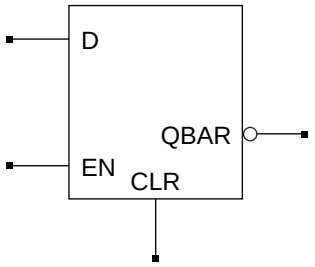
Input

CLR, EN, D

Output

Q

LDCI



Function

Active High Latch with Active High Clear and Active Low Output

Truth Table

EN	CLR	$QBAR_{n+1}$
X	1	1
1	0	!D
0	0	QBAR

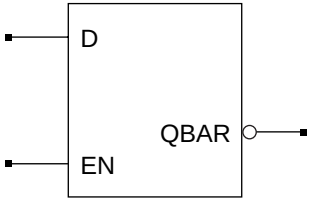
Input

CLR, EN, D

Output

QBAR

LDI



Function

Active High Latch with Active Low Output

Truth Table

EN	$QBAR_{n+1}$
0	QBAR
1	!D

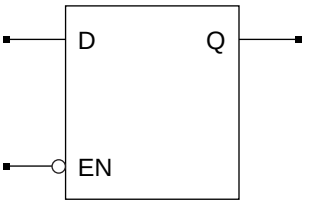
Input

EN, D

Output

QBAR

LDL



Function

Active Low Latch

Truth Table

EN	Q_{n+1}
0	D
1	Q

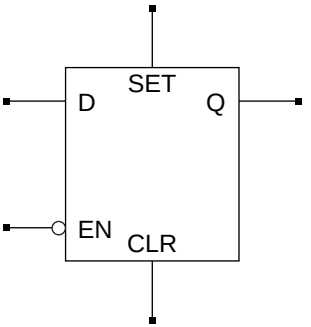
Input

EN, D

Output

Q

LDLB



Function

Active Low Latch with Active High Set and Clear

Truth Table

EN	SET	CLR	Q_{n+1}
X	1	0	1
X	X	1	0
0	0	0	D
1	0	0	Q

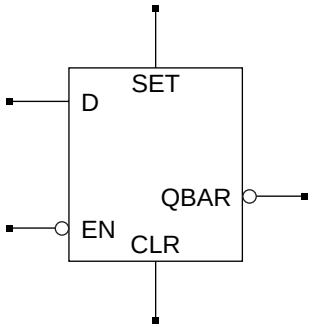
Input

CLR, SET, EN, D

Output

Q

LDLBI



Function

Active Low Latch with Active High Set and Clear and Active Low Output

Truth Table

EN	SET	CLR	$QBAR_{n+1}$
X	1	0	0
X	X	1	1
0	0	0	!D
1	0	0	QBAR

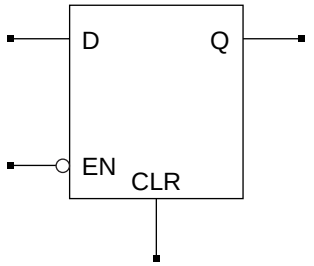
Input

CLR, SET, EN, D

Output

QBAR

LDLC



Function

Active Low Latch with Active High Clear

Truth Table

EN	CLR	Q_{n+1}
X	1	0
0	0	D
1	0	Q

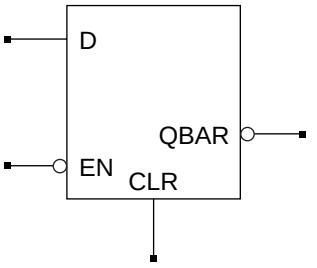
Input

CLR, EN, D

Output

Q

LDLCI



Function

Active Low Latch with Active High Clear and Active Low Output

Truth Table

EN	CLR	$QBAR_{n+1}$
X	1	1
0	0	!D
1	0	QBAR

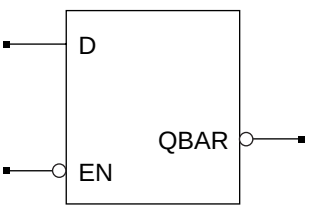
Input

CLR, EN, D

Output

QBAR

LDLI



Function

Active Low Latch with Active Low Output

Truth Table

EN	$QBAR_{n+1}$
0	!D
1	QBAR

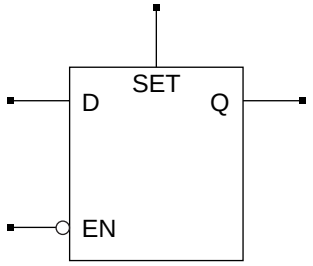
Input

EN, D

Output

QBAR

LDLS



Function

Active Low Latch with Active High Set

Truth Table

EN	SET	Q_{n+1}
X	1	1
0	0	D
1	0	Q

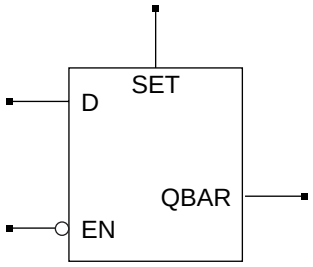
Input

SET, EN, D

Output

Q

LDLSI



Function

Active Low Latch with Active High Set and Active Low Output

Truth Table

EN	SET	$QBAR_{n+1}$
X	1	0
0	0	!D
1	0	QBAR

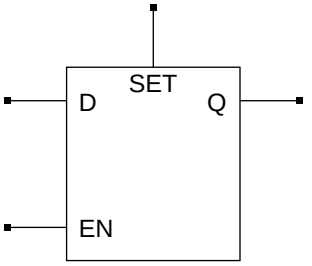
Input

SET, EN, D

Output

QBAR

LDS



Function

Active High Latch with Active High Set

Truth Table

EN	SET	Q_{n+1}
X	1	1
0	0	Q
1	0	D

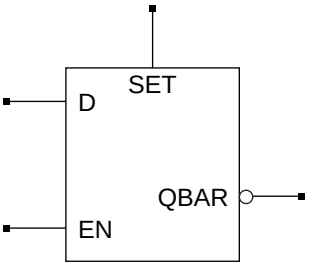
Input

SET, EN, D

Output

Q

LDSI



Function

Active High Latch with Active High Set and Active Low Output

Truth Table

EN	SET	$QBAR_{n+1}$
X	1	0
0	0	QBAR
1	0	!D

Input

SET, EN, D

Output

QBAR

3

Input/Output Cells

This section describes input buffers, global buffers, output buffers and bidirectional buffers.

Input Buffers

A500K input buffers have the following features:

- CMOS voltage levels for 2.5 V and 3.3 V.
- Optional pull-up resistor.
- ESD protection circuitry.
- Latch-up protection circuitry.

Input Buffer Naming Conventions

Names for the input buffers are composed of up to 4 parts:

- A base name indicating the type of input buffer (IB for input with positive pad logic, IBN with negative pad logic).
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- An optional one character code (U) designating a pull-up resistor. When the buffer has no resistor, this code is omitted.

For Example:

IB25 - An input buffer with 2.5 CMOS voltage levels and no pull-up resistor.

IB33U - An input buffer with 3.3 CMOS voltage levels and pull-up resistor.

Global Buffers

Global buffers are provided for use with low skew, high fanout nets, such as, clock and reset. They can be either driven from a pad or internally. If a global buffer is used internally, the pad can be used for other input signals.

A500K global buffers have the following features:

- 2.5 or 3.3 CMOS voltage levels.
- Optional pull-up resistor.
- ESD protection circuitry.

- Latch-up protection circuitry.
- Multiplexed input for external or internal drive.

Global Buffer Naming Conventions

Four types of global buffers are available: standard global input buffers (GL), global buffers with independent input buffers (GLIB), global multiplexed input buffers (GLMIB) and global buffers with internal connection only (GLINT).

Global buffer names are composed of up to four parts:

- The name base indicating the type of buffer (GL, GLIB, GLMIB for external buffers, GLINT for an internal connected global buffer).
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- An optional one character code (U) designating a pull-up resistor (except GLINT). When there is no resistor, this code is omitted.

For Example:

GL25U - Global input buffer with 2.5 CMOS voltage levels and pull-up resistor.

GLIB33 - Global buffer with 3.3 CMOS voltage levels input buffer and global buffer with input A.

GLMIB33U - Global multiplexed input buffer with 3.3 CMOS voltage levels, active low enable input and pull-up resistor.

Output Buffers

A500K output buffers have the following features:

- Optional PCI compliance with PCI 2.1 Component Specification (3.3 Voltage pad only).
- Selectable drive strengths.
- Selectable slew rates.
- Optional three-state functionality.
- ESD protection circuitry.
- Latch-up protection circuitry.

Output Buffer Naming Conventions

Names for the output buffers are composed of up to five parts:

- The name base indicating the type of output buffer (OB for output buffer, OTB for three-state output buffer).
- An optional one character code (L) designating an active low enable input for the OTB output buffer. The code is omitted for the active high enable input.
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.

- A code indicating the drive strength (2.5 Volt pad: L for 1 mA, H for 3.5 mA; 3.3 Volt pad: L for 5 mA and P for PCI compliant 10 mA).
- A one character code indicating the slew rate (L for low 25 mA/ns, N for nominal 50 mA/ns, and H for high 100 mA/ns).

For Example:

OB25HN - 2.5 Volt output buffer, high drive strengths and nominal slew rate.

OTB33LH - Three-state output buffer, low drive strengths, high slew rate.

OB33PL - PCI compliant output buffer (= high drive strengths) and low slew rate.

Bidirectional Buffers

A500K bidirectional buffers have all the features of both the input buffers and the output buffers:

- 2.5 and 3.3 CMOS input voltage levels.
- Optional pull-up resistor.
- Optional PCI compliance with PCI 2.1 Component Specification (3.3 Voltage pad only).
- Selectable drive strengths.
- Selectable slew rates.
- Three-state functionality.
- ESD protection circuitry.
- Latch-up protection circuitry.

Bidirectional Buffer Naming Conventions

Names for the bidirectional buffers are composed of up to seven parts:

- The name base IOB identifying the buffer as a bidirectional buffer.
- An optional one character code (L) designating an active low enable input for the IOB output buffer part. The code is omitted for the active high enable input.
- The number code 25 or 33 indicating a 2.5 or 3.3 voltage level.
- A two character code indicating low power pad voltage (LP).
- A code indicating the drive strength (2.5 Volt pad: L for 1 mA, H for 3.5 mA; 3.3 Volt pad: L for 5 mA and P for PCI compliant 10 mA).
- A one character code indicating the slew rate (L for low 25 mA/ns, N for nominal 50 mA/ns, and H for high 100 mA/ns).
- An optional one character code (U) designating a pull-up resistor. When there is no resistor, this code is omitted.

For Example:

IOB25LLU - A 2.5 Volt bidirectional buffer with low drive strength, low slew rate and a pull-up resistor.

IOB33PHU - A 3.3 Volt PCI compliant bidirectional buffer with high slew rate and a pull-up resistor.

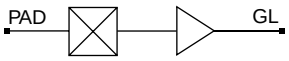
IOBL33LN - A 3.3 Volt bidirectional buffer with active low enable input, low drive strength and normal slew rate.

Truth Table Symbol Descriptions

Combinational truth tables use the following symbols:

- 1 - indicates logic level one.
- 0 - indicates logic level zero.
- A - indicates internal input port.
- NC - indicates not connected.
- PAD - indicates external port.
- X - indicates either logic level one or zero (don't care).
- Z - indicates three-state logic level (high resistance).

GLx



Function

Global Input Buffer

Truth Table

Input	Output
PAD	GL
0	0
1	1

Input

PAD

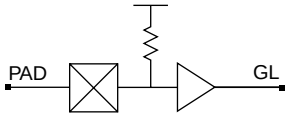
Output

GL

Available GLx Macro Types

Name	Description
GL25	2.5 Volt CMOS input levels
GL33	3.3 Volt CMOS input levels
GL25LP	2.5 Volt CMOS input levels, low power

GLxU



Function

Global Input Buffer with Pull-up Resistor

Truth Table

Input	Output
PAD	GL
0	0
1	1
NC	1

Input

PAD

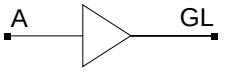
Output

GL

Available GLxU Macro Types

Name	Description
GL25U	2.5 Volt CMOS input levels, with pull-up resistor
GL33U	3.3 Volt CMOS input levels, with pull-up resistor
GL25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor

GLINT



Function

Global Buffer with Internal Connection

Truth Table

Input	Output
A	GL
1	1
0	0

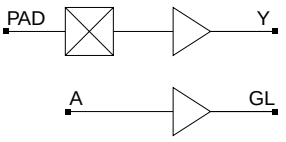
Input

A

Output

GL

GLIBx



Function

Global Input Buffer with Independent Input Buffer

Truth Table

Input	Output	Input	Output
PAD	Y	A	GL
1	1	1	1
0	0	0	0

Input

PAD, A

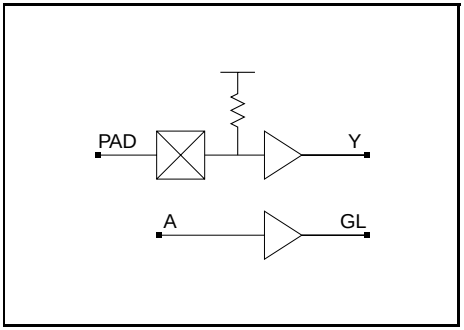
Output

Y, GL

Available GLIBx Macro Types

Name	Description
GLIB25	2.5 Volt CMOS input levels
GLIB33	3.3 Volt CMOS input levels
GLIB25LP	2.5 Volt CMOS input levels, low power

GLIBxU



Function

Global Input Buffer with Independent Input Buffer and Pull-up Resistor

Truth Table

Input	Output	Input	Output
PAD	Y	A	GL
1	1	1	1
0	0	0	0
NC	1		

Input

PAD, A

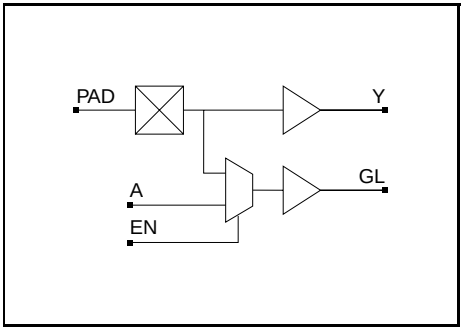
Output

Y, GL

Available GLIBxU Macro Types

Name	Description
GLIB25U	2.5 Volt CMOS input levels, with pull-up resistor
GLIB33U	3.3 Volt CMOS input levels, with pull-up resistor
GLIB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor

GLMIBx



Function

Global Multiplexed Input Buffer

Truth Table

Input	Output
PAD	Y
1	1
0	0

Truth Table

Input			Output
PAD	A	EN	GL
0	X	0	0
1	X	0	1
X	1	1	1
X	0	1	0

Input

PAD, A, EN

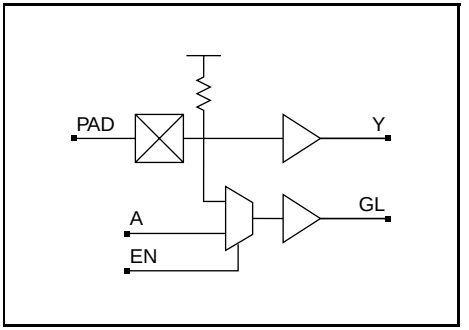
Output

Y, GL

Available GLMIBx Macro Types

Name	Description
GLMIB25	2.5 Volt CMOS input levels
GLMIB33	3.3 Volt CMOS input levels
GLMIB25LP	2.5 Volt CMOS input levels, low power

GLMIBxU



Function

Global Multiplexed Input Buffer with Pull-up Resistor

Input

PAD, A, EN

Output

Y, GL

Truth Table

Input	Output
PAD	Y
1	1
0	0
NC	1

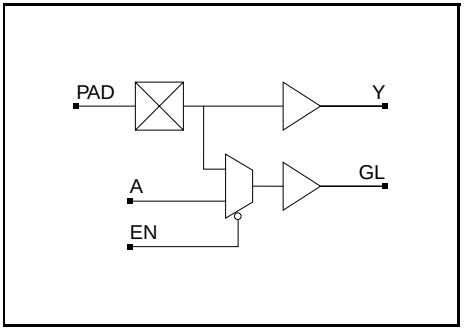
Truth Table

Input			Output
PAD	A	EN	GL
0	X	0	0
1	X	0	1
X	1	1	1
X	0	1	0
NC	X	0	1

Available GLMIBxU Macro Types

Name	Description
GLMIB25U	2.5 Volt CMOS input levels, with pull-up resistor
GLMIB33U	3.3 Volt CMOS input levels, with pull-up resistor
GLMIB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor

GLMIBLx



Function

Global Multiplexed Input Buffer with Active Low Enable

Input

PAD, A, EN

Output

Y, GL

Truth Table

Input	Output
PAD	Y
1	1
0	0

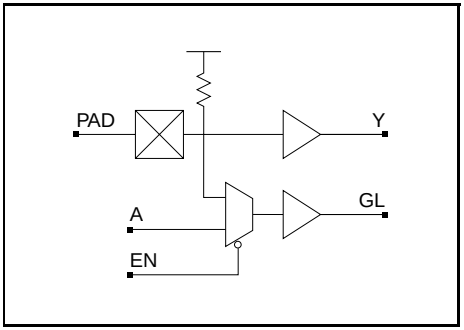
Truth Table

Input			Output
PAD	A	EN	GL
X	0	0	0
X	1	0	1
1	X	1	1
0	X	1	0

Available GLMIBLxU Macro Types

Name	Description
GLMIBL25	2.5 Volt CMOS input levels
GLMIBL33	3.3 Volt CMOS input levels
GLMIBL25LP	2.5 Volt CMOS input levels, low power

GLMIBLxU



Function

Global Multiplexed Input Buffer with Active Low Enable and Pull-up Resistor

Truth Table

Input	Output
PAD	Y
0	0
1	1
NC	1

Truth Table

Input			Output
PAD	A	EN	GL
X	0	0	0
X	1	0	1
1	X	1	1
0	X	1	0
NC	X	1	1

Input

PAD, A, EN

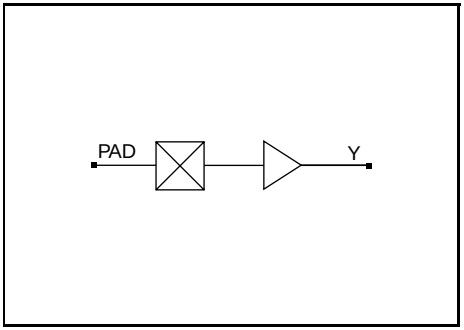
Output

Y, GL

Available GLMIBLxU Macro Types

Name	Description
GLMIBL25U	2.5 Volt CMOS input levels, with pull-up resistor
GLMIBL33U	3.3 Volt CMOS input levels, with pull-up resistor
GLMIBL25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor

IBx



Function

Input Buffer

Truth Table

Input	Output
PAD	Y
0	0
1	1

Input

PAD

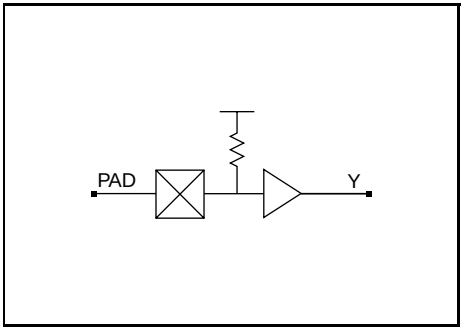
Output

Y

Available IBx Macro Types

Name	Description
IB25	2.5 Volt CMOS input levels
IB33	3.3 Volt CMOS input levels
IB25LP	2.5 Volt CMOS input levels, low power

IBxU



Function

Input Buffer with Pull-up Resistor

Truth Table

Input	Output
PAD	Y
0	0
1	1
NC	1

Input

PAD

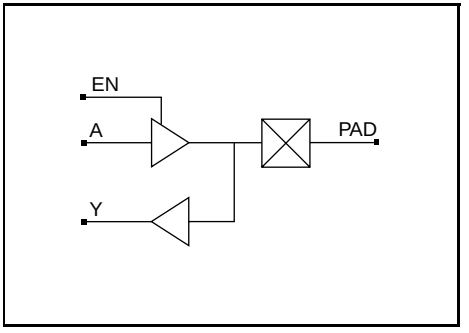
Output

Y

Available IBxU Macro Types

Name	Description
IB25U	2.5 Volt CMOS input levels, with pull-up resistor
IB33U	3.3 Volt CMOS input levels, with pull-up resistor
IB25LPU	2.5 Volt CMOS input levels, low power, with pull-up resistor

IOB25x



Function

Bi-Directional Buffer

Truth Table

Input			Output	
EN	A	PAD	PAD	Y
1	X	X	A	A
0	X	X	X	PAD

Input

EN, A, PAD

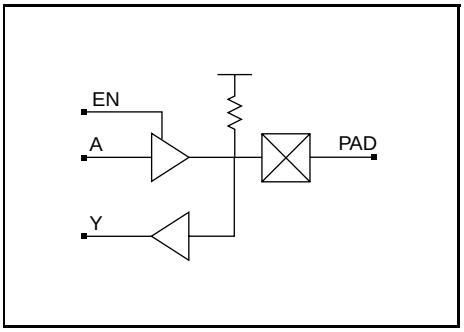
Output

PAD, Y

Available IOB25x Macro Types

Name	Description
IOB25HH	2.5 Volt CMOS input levels, high drive strength, high slew rate
IOB25HL	2.5 Volt CMOS input levels, high drive strength, low slew rate
IOB25HN	2.5 Volt CMOS input levels, high drive strength, normal slew rate
IOB25LH	2.5 Volt CMOS input levels, low drive strength, high slew rate
IOB25LL	2.5 Volt CMOS input levels, low drive strength, low slew rate
IOB25LN	2.5 Volt CMOS input levels, low drive strength, normal slew rate

IOB25xU



Function

Bi-Directional Buffer with Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Input

EN, A, PAD

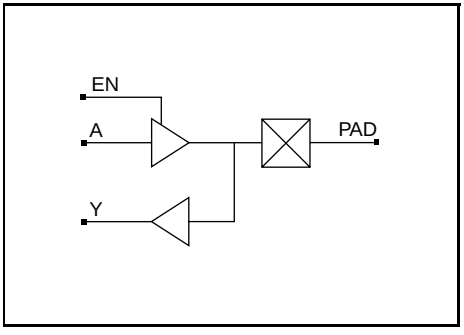
Output

PAD, Y

Available IOB25xU Macro Types

Name	Description
IOB25HHU	2.5 Volt CMOS input levels, high drive strength, high slew rate, with pull-up resistor
IOB25HLU	2.5 Volt CMOS input levels, high drive strength, low slew rate, with pull-up resistor
IOB25HNU	2.5 Volt CMOS input levels, high drive strength, normal slew rate, with pull-up resistor
IOB25LHU	2.5 Volt CMOS input levels, low drive strength, high slew rate, with pull-up resistor
IOB25LLU	2.5 Volt CMOS input levels, low drive strength, low slew rate, with pull-up resistor
IOB25LNU	2.5 Volt CMOS input levels, low drive strength, normal slew rate, with pull-up resistor

IOB25LPx



Function

Bi-Directional Buffer (Low Power)

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	A	A
0	X	X	X	PAD

Input

EN, A, PAD

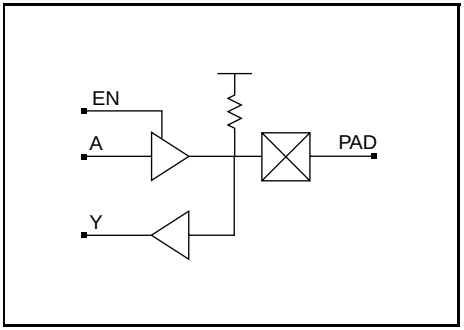
Output

PAD, Y

Available IOB25LPx Macro Types

Name	Description
IOB25LPHH	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate
IOB25LPHL	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate
IOB25LPHN	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate
IOB25LPLH	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate
IOB25LPLL	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate
IOB25LPLN	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate

IOB25LPxU



Function

Bi-Directional Buffer with Low Power and Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Input

EN, A, PAD

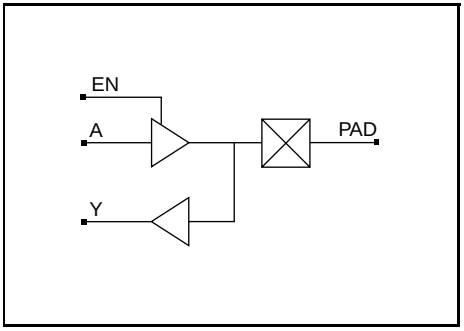
Output

PAD, Y

Available IOB25LPxU Macro Types

Name	Description
IOB25LPHHU	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate, with pull-up resistor
IOB25LPHLU	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate, with pull-up resistor
IOB25LPHNU	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate, with pull-up resistor
IOB25LPLHU	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate, with pull-up resistor
IOB25LPLLU	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate, with pull-up resistor
IOB25LPLNU	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate, with pull-up resistor

IOB33x



Function

Bi-Directional Buffer

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	A	A
0	X	X	X	PAD

Input

EN, A, PAD

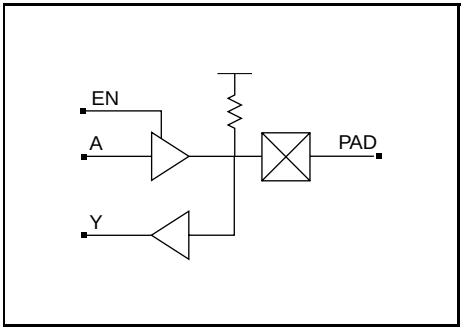
Output

PAD, Y

Available IOB33x Macro Types

Name	Description
IOB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
IOB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
IOB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
IOB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
IOB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
IOB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

IOB33xU



Function

Bi-Directional Buffer with Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	A	A
0	X	X	X	PAD
0	X	NC	NC	1

Input

EN, A, PAD

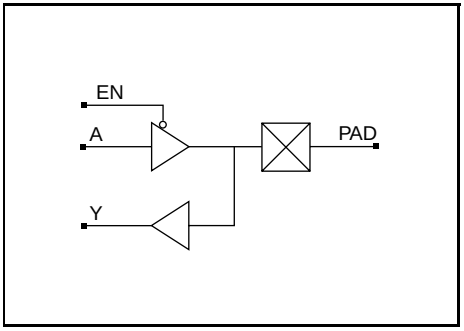
Output

PAD, Y

Available IOB33xU Macro Types

Name	Description
IOB33LHU	3.3 Volt CMOS input levels, low strength drive, high slew rate, with pull-up resistor
IOB33LLU	3.3 Volt CMOS input levels, low strength drive, low slew rate, with pull-up resistor
IOB33LNU	3.3 Volt CMOS input levels, low strength drive, normal slew rate, with pull-up resistor
IOB33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew rate, with pull-up resistor
IOB33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew rate, with pull-up resistor
IOB33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew rate, with pull-up resistor

IOBL25x



Function

Bi-Directional Buffer with Active Low Enable

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A

Input

EN, A, PAD

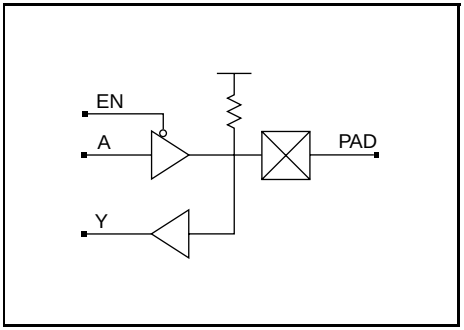
Output

PAD, Y

Available IOBL25x Macro Types

Name	Description
IOBL25HH	2.5 Volt CMOS input levels, high drive strength, high slew rate
IOBL25HL	2.5 Volt CMOS input levels, high drive strength, low slew rate
IOBL25HN	2.5 Volt CMOS input levels, high drive strength, normal slew rate
IOBL25LH	2.5 Volt CMOS input levels, low drive strength, high slew rate
IOBL25LL	2.5 Volt CMOS input levels, low drive strength, low slew rate
IOBL25LN	2.5 Volt CMOS input levels, low drive strength, normal slew rate

IOBL25xU



Function

Bi-Directional Buffer with Active Low Enable and Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Input

EN, A, PAD

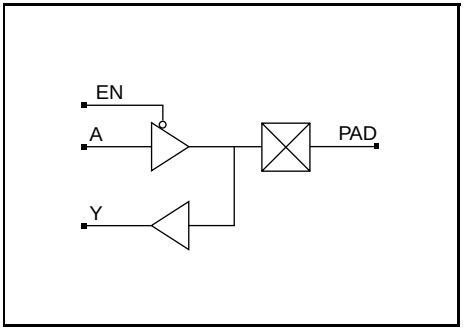
Output

PAD, Y

Available IOBL25xU Macro Types

Name	Description
IOBL25HHU	2.5 Volt CMOS input levels, high drive strength, high slew rate, with pull-up resistor
IOBL25HLU	2.5 Volt CMOS input levels, high drive strength, low slew rate, with pull-up resistor
IOBL25HNU	2.5 Volt CMOS input levels, high drive strength, normal slew rate, with pull-up resistor
IOBL25LHU	2.5 Volt CMOS input levels, low drive strength, high slew rate, with pull-up resistor
IOBL25LLU	2.5 Volt CMOS input levels, low drive strength, low slew rate, with pull-up resistor
IOBL25LNU	2.5 Volt CMOS input levels, low drive strength, normal slew rate, with pull-up resistor

IOBL25LPx



Function

Bi-Directional Buffer with Active Low Enable (Low Power)

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A

Input

EN, A, PAD

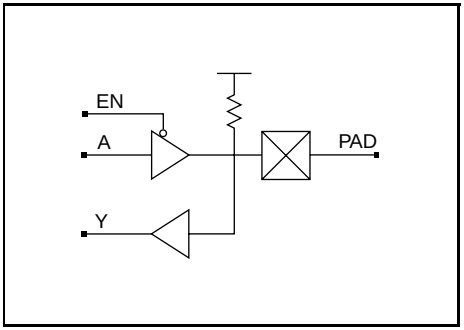
Output

PAD, Y

Available IOBL25LPx Macro Types

Name	Description
IOBL25LPHH	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate
IOBL25LPHL	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate
IOBL25LPHN	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate
IOBL25LPLH	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate
IOBL25LPLL	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate
IOBL25LPLN	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate

IOBL25LPxU



Function

Bi-Directional Buffer with Active Low Enable, Low Power, and Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Input

EN, A, PAD

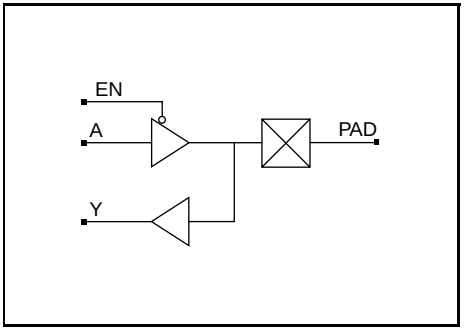
Output

PAD, Y

Available IOBL25LPxU Macro Types

Name	Description
IOBL25LPHHU	2.5 Volt CMOS input levels, low power, high drive strength, high slew rate, with pull-up resistor
IOBL25LPHLU	2.5 Volt CMOS input levels, low power, high drive strength, low slew rate, with pull-up resistor
IOBL25LPHNU	2.5 Volt CMOS input levels, low power, high drive strength, normal slew rate, with pull-up resistor
IOBL25LPLHU	2.5 Volt CMOS input levels, low power, low drive strength, high slew rate, with pull-up resistor
IOBL25LPLLU	2.5 Volt CMOS input levels, low power, low drive strength, low slew rate, with pull-up resistor
IOBL25LPLNU	2.5 Volt CMOS input levels, low power, low drive strength, normal slew rate, with pull-up resistor

IOBL33x



Function

Bi-Directional Buffer with Active Low Enable

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A

Input

EN. PAD, A

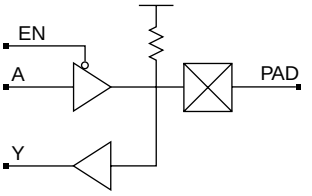
Output

PAD, Y

Available IOBL33x Macro Types

Name	Description
IOBL33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
IOBL33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
IOBL33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
IOBL33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
IOBL33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
IOBL33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

IOBL33xU



Function

Bi-Directional Buffer with Active Low Enable and Pull-up Resistor

Truth Table

Input			Output	
EN	**A**	**PAD**	**PAD**	**Y**
1	X	X	X	PAD
0	X	X	A	A
1	X	NC	NC	1

Input

EN. PAD, A

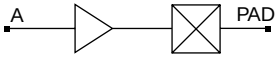
Output

PAD, Y

Available IOBL33xU Macro Types

Name	Description
IOBL33LHU	3.3 Volt CMOS input levels, low strength drive, high slew rate, with pull-up resistor
IOBL33LLU	3.3 Volt CMOS input levels, low strength drive, low slew rate, with pull-up resistor
IOBL33LNU	3.3 Volt CMOS input levels, low strength drive, normal slew rate, with pull-up resistor
IOBL33PHU	3.3 Volt CMOS input levels, PCI compliant, high slew rate, with pull-up resistor
IOBL33PLU	3.3 Volt CMOS input levels, PCI compliant, low slew rate, with pull-up resistor
IOBL33PNU	3.3 Volt CMOS input levels, PCI compliant, normal slew rate, with pull-up resistor

OB25x



Function

Output Buffer

Truth Table

Input	Output
A	**PAD**
0	0
1	1

Input

A

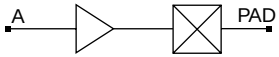
Output

PAD

Available OB25x Macro Types

Name	Description
OB25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OB25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OB25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OB25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OB25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OB25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OB25LPx



Function

Output Buffer (Low Power)

Truth Table

Input	Output
A	**PAD**
0	0
1	1

Input

A

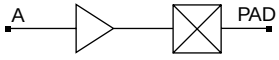
Output

PAD

Available OB25LPx Macro Types

Name	Description
OB25LPHH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OB25LPHL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OB25LPHN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OB25LPLH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OB25LPLL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OB25LPLN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OB33x



Function

Output Buffer

Truth Table

Input	Output
A	**PAD**
0	0
1	1

Input

A

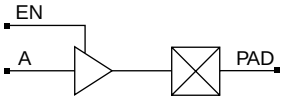
Output

PAD

Available OB33x Macro Types

Name	Description
OB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

OTB25x



Function

Three State Output Buffer

Truth Table

Input		Output
EN	**A**	**PAD**
0	X	Z
1	1	1
1	0	0

Input

EN, A

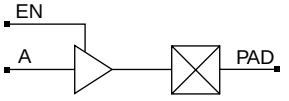
Output

PAD

Available OTB25x Macro Types

Name	Description
OTB25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OTB25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OTB25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OTB25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OTB25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OTB25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OTB25LPx



Function

Three State Output Buffer (Low Power)

Truth Table

Input		Output
EN	**A**	**PAD**
0	X	Z
1	1	1
1	0	0

Input

EN, A

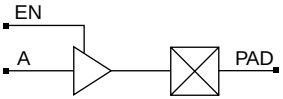
Output

PAD

Available OTB25LPx Macro Types

Name	Description
OTB25LPLH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OTB25LPLL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OTB25LPLN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OTB25LPLH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OTB25LPLL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OTB25LPLN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OTB33x



Function

Three State Output Buffer

Truth Table

Input		Output
EN	**A**	**PAD**
0	X	Z
1	1	1
1	0	0

Input

EN, A

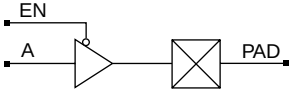
Output

PAD

Available OTB33x Macro Types

Name	Description
OTB33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OTB33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OTB33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OTB33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OTB33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OTB33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

OTBL25x



Function

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	**A**	**PAD**
0	0	0
0	1	1
1	X	Z

Input

EN, A

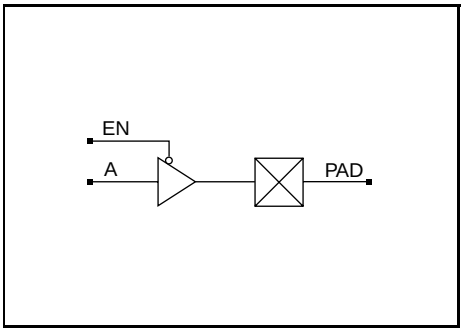
Output

PAD

Available OTBL25x Macro Types

Name	Description
OTBL25HH	2.5 Volt CMOS input levels, high strength drive, high slew rate
OTBL25HL	2.5 Volt CMOS input levels, high strength drive, low slew rate
OTBL25HN	2.5 Volt CMOS input levels, high strength drive, normal slew rate
OTBL25LH	2.5 Volt CMOS input levels, low strength drive, high slew rate
OTBL25LL	2.5 Volt CMOS input levels, low strength drive, low slew rate
OTBL25LN	2.5 Volt CMOS input levels, low strength drive, normal slew rate

OTBL25LPx



Function

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	**A**	**PAD**
0	0	0
0	1	1
1	X	Z

Input

EN, A

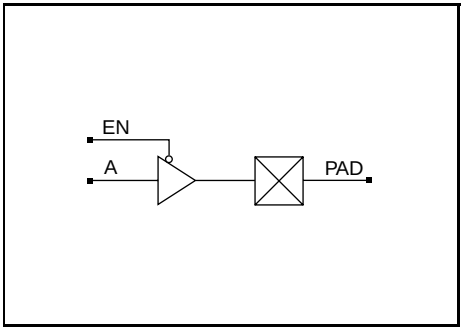
Output

PAD

Available OTBL25LPx Macro Types

Name	Description
OTBL25LPLH	2.5 Volt CMOS input levels, low power, high strength drive, high slew rate
OTBl25LPLL	2.5 Volt CMOS input levels, low power, high strength drive, low slew rate
OTBL25LPLN	2.5 Volt CMOS input levels, low power, high strength drive, normal slew rate
OTBL25LPPH	2.5 Volt CMOS input levels, low power, low strength drive, high slew rate
OTBL25LPPL	2.5 Volt CMOS input levels, low power, low strength drive, low slew rate
OTBL25LPPN	2.5 Volt CMOS input levels, low power, low strength drive, normal slew rate

OTBL33x



Function

Three State Output Buffer with Active Low Enable

Truth Table

Input		Output
EN	**A**	**PAD**
0	0	0
0	1	1
1	X	Z

Input

EN, A

Output

PAD

Available OTBL33X Macro Types

Name	Description
OTBL33LH	3.3 Volt CMOS input levels, low strength drive, high slew rate
OTBL33LL	3.3 Volt CMOS input levels, low strength drive, low slew rate
OTBL33LN	3.3 Volt CMOS input levels, low strength drive, normal slew rate
OTBL33PH	3.3 Volt CMOS input levels, PCI compliant, high slew rate
OTBL33PL	3.3 Volt CMOS input levels, PCI compliant, low slew rate
OTBL33PN	3.3 Volt CMOS input levels, PCI compliant, normal slew rate

4

Memory Cells

Embedded memory blocks in the A500K family can be configured as FIFO or static RAM with the following features:

- basic block size is 256 word by 9 bit.
- FIFO includes complete control logic.
- static RAM with independent read and write ports.

Naming Convention for RAMs

RAM model names consist of up to four parts:

- A base name indicating the type and size (RAM256x9)
- A one character code designating the write port as asynchronous (A) or synchronous (S).
- A one or two character code designating the read port as asynchronous (A) or synchronous registered (SR) or synchronous transparent (ST).
- An optional one character code designating parity (P) generated.

For example: RAM256x9SAP is a 256-word by 9-bit RAM with synchronous write and asynchronous read ports using the generate parity feature.

SRAM Interface Signals

The illustration and table below describe basic embedded SRAM interface signals.

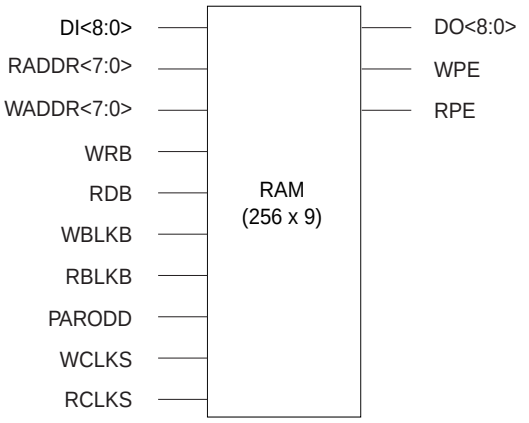


Table 4-1: SRAM Signal Descriptions

SRAM Signal	Bits	In/Out	Description
DI<8:0>	9	IN	Input data bits <8:0>, <8> can be used for parity in
RADDR<7:0>	8	IN	Read address
WADDR<7:0>	8	IN	Write address
WRB	1	IN	Negative true write pulse
RDB	1	IN	Negative true read pulse
WBLKB	1	IN	Negative true write block select
RBLKB	1	IN	Negative true read block select
PARODD	1	IN	Selects odd parity generation/detect when high, even when low
WCLKS	1	IN	Write clock used in synchronous mode on write side
RCLKS	1	IN	Write clock used in synchronous mode on read side
DO<8:0>	9	OUT	Output data bits <8:0>, <8> can be used for parity out
WPE	1	OUT	Write parity error flag
RPE	1	OUT	Read parity error flag

Naming Convention for FIFOs

FIFO model names consist of up to four parts:

- A base name indicating the type and size (FIFO256x9)
- A one character code designating the write port as asynchronous (A) or synchronous (S).
- A one or two character code designating the read port as asynchronous (A) or synchronous registered (SR) or synchronous transparent (ST).
- An optional one character code designating parity (P) generated.

For example: FIFO256x9SSRP is a 256-word by 9-bit FIFO with synchronous write and synchronous read ports (synchronous to separate clocks named RCLKS and WCLKS), has registered outputs and uses the generate parity feature.

FIFO Interface Signals

This illustration and the table below describe FIFO interface signals.

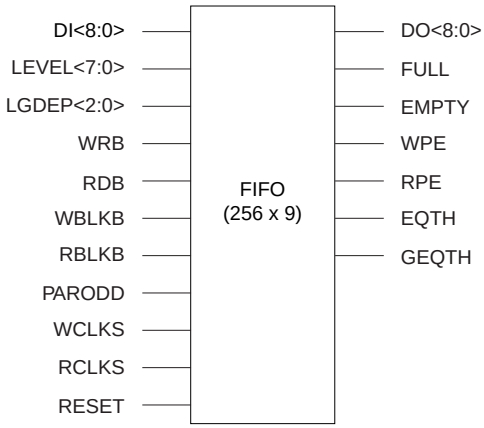
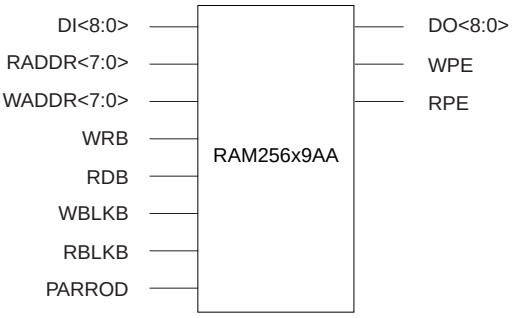


Table 4-2: FIFO Signal Descriptions

FIFO Signal	Bits	In/Out	Description
DI<8:0>	9	IN	Input data bits <8:0>, <8> can be used for parity in
LEVEL<7:0>	8	IN	Reference signal for the generation of the EQTH and GEQTH flags
LGDEP<2:0>	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
WRB	1	IN	Negative true write pulse
RDB	1	IN	Negative true read pulse
WBLKB	1	IN	Negative true write block select
RBLKB	1	IN	Negative true read block select
PARODD	1	IN	Selects odd parity generation/detect when high, even when low
WCLKS	1	IN	Write clock used in synchronous mode on write side
RCLKS	1	IN	Write clock used in synchronous mode on read side
RESET	1	IN	Negative true reset for FIFO pointers
DO<8:0>	9	OUT	Output data bits <8:0>, <8> can be used for parity out
FULL	2	OUT	FIFO flag. FULL prevents write. EMPTY prevents read
EMPTY	1	OUT	FIFO flag. EMPTY prevents read
WPE	1	OUT	Write parity error flag
RPE	1	OUT	Read parity error flag
EQTH	1	OUT	EQTH is true when the FIFO holds (LEVEL) words
GEQTH	1	OUT	GEQTH is true when the FIFO holds (LEVEL) words or more

RAM256x9AA



Function

Asynchronous Write/Asynchronous Read RAM with Parity Checking

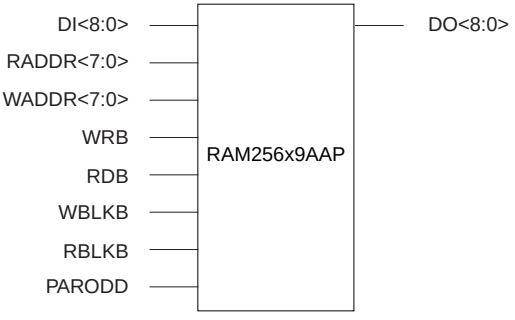
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, PARROD

Output

DO, WPE, RPE

RAM256x9AAP



Function

Asynchronous Write/Asynchronous Read RAM with Parity Generation

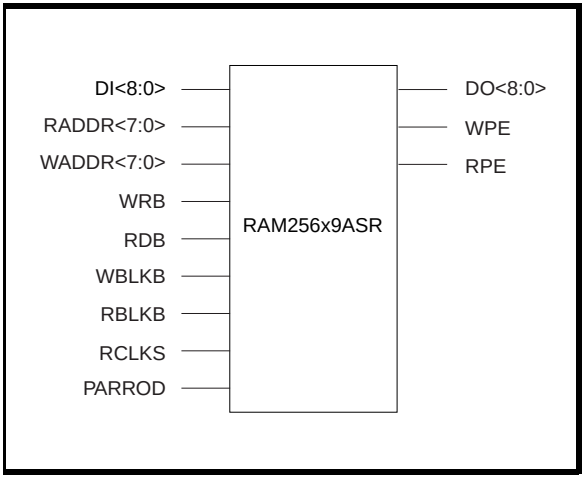
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, PARROD

Output

DO

RAM256x9ASR



Function

Asynchronous Write/Synchronous Read RAM with Registered Output and Parity Checking

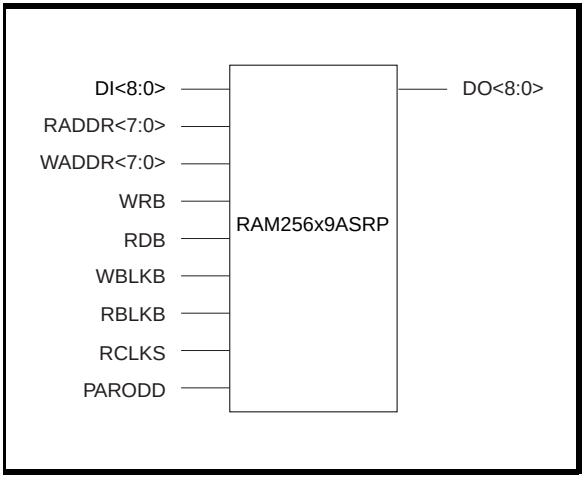
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, RCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9ASRP



Function

Asynchronous Write/Synchronous Read RAM with Registered Output and Parity Generation

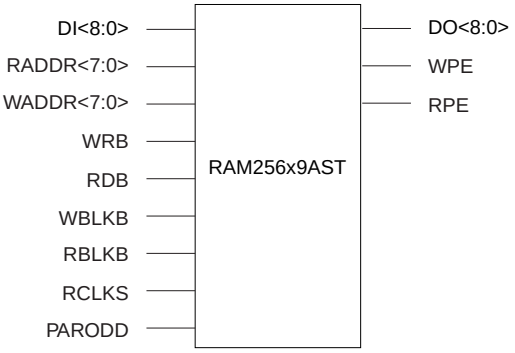
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, RCLKS, PARROD

Output

DO

RAM256x9AST



Function

Asynchronous Write/Synchronous Read RAM with Transparent Output and Parity Checking

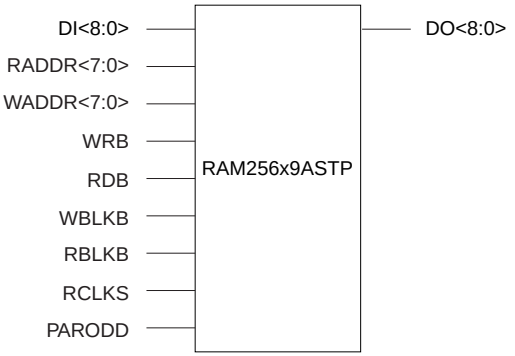
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, RCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9ASTP



Function

Asynchronous Write/Synchronous Read RAM with Transparent Output and Parity Generation

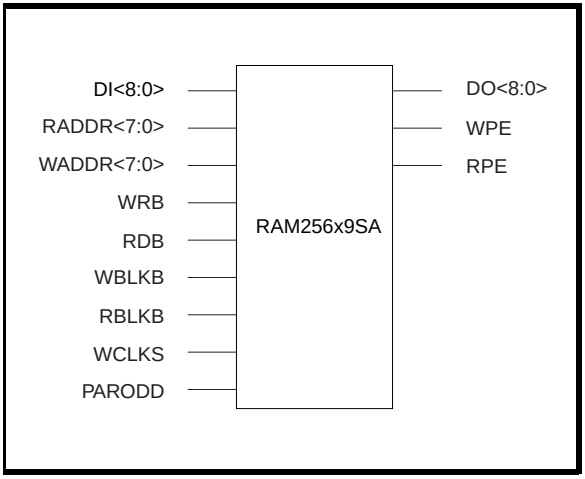
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, RCLKS, PARROD

Output

DO

RAM256x9SA



Function

Synchronous Write/Asynchronous Read RAM with Parity Checking

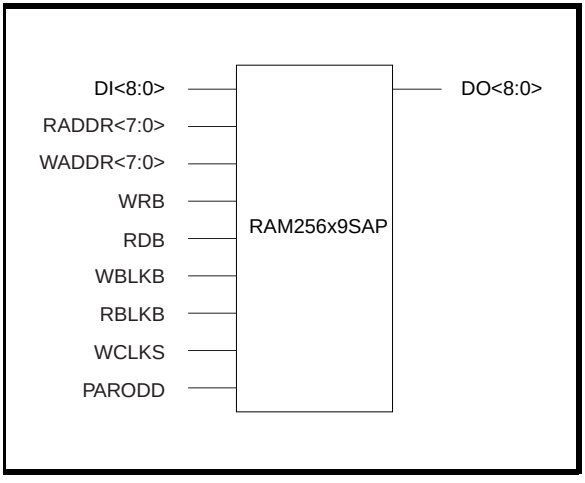
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9SAP



Function

Synchronous Write/Asynchronous Read RAM with Parity Generation

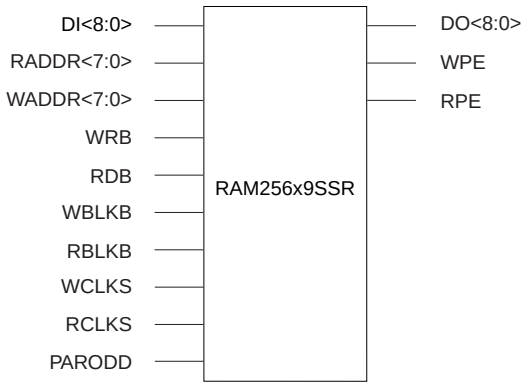
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, PARROD

Output

DO

RAM256x9SSR



Function

Synchronous Write/Synchronous Read RAM with Registered Output and Parity Checking

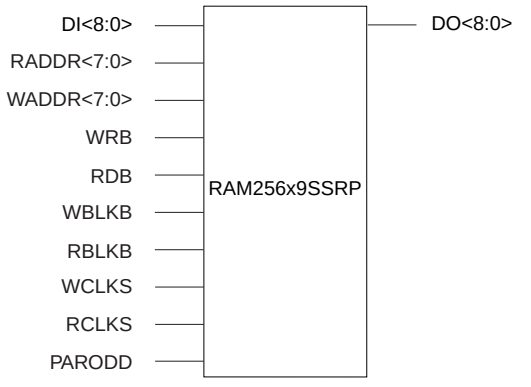
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9SSRP



Function

Synchronous Write/Synchronous Read RAM with Registered Output and Parity Generation

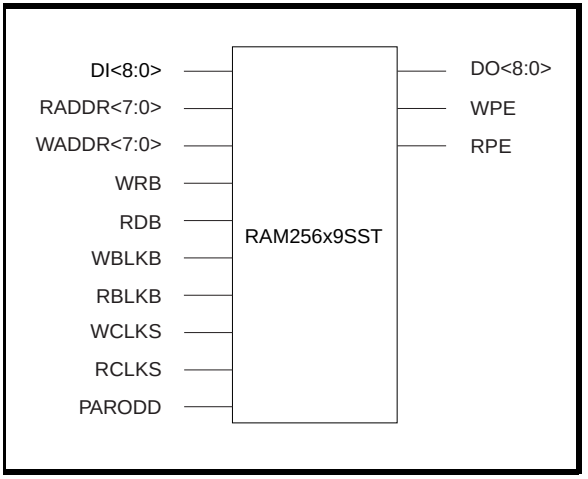
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, PARROD

Output

DO

RAM256x9SST



Function

Synchronous Write/Synchronous Read RAM with Transparent Output and Parity Checking

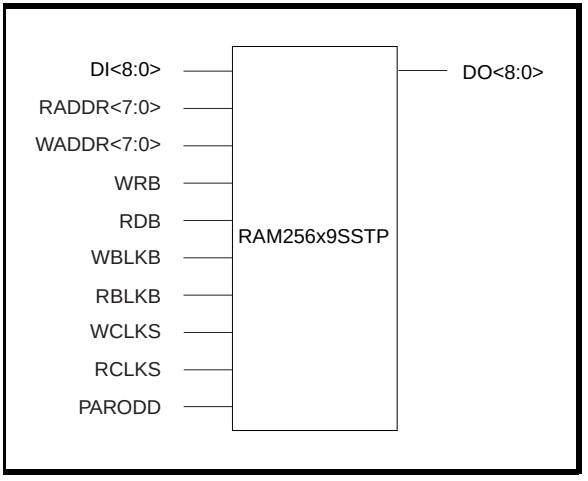
Input

DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, PARROD

Output

DO, WPE, RPE

RAM256x9SSTP



Function

Synchronous Write/Synchronous Read RAM with Transparent Output and Parity Generation

Input

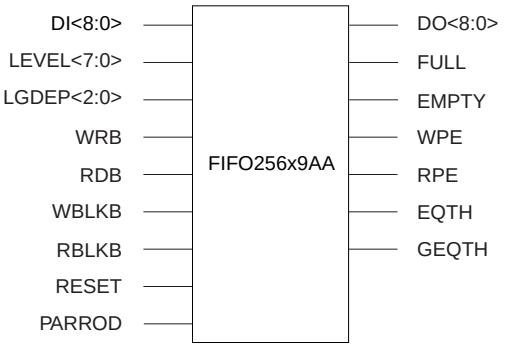
DI, RADDR, WADDR, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, PARROD

Output

DO

Memory Cells, FIFO

FIFO256x9AA



Function

Asynchronous Write/Asynchronous Read FIFO with Parity Checking

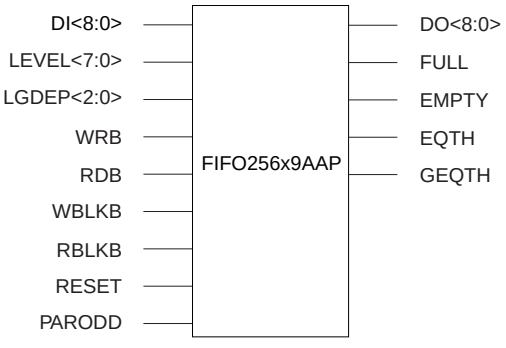
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9AAP



Function

Asynchronous Write/Asynchronous Read FIFO with Parity Generation

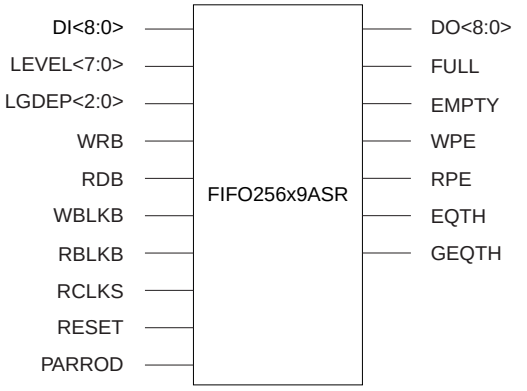
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9ASR



Function

Asynchronous Write/Synchronous Read FIFO with Registered Output and Parity Checking

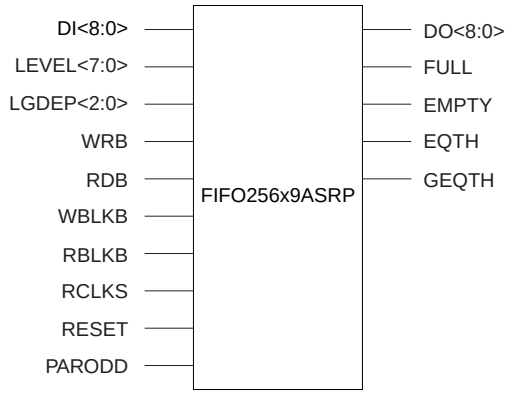
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9ASRP



Function

Asynchronous Write/Synchronous Read FIFO with Registered Output and Parity Generation

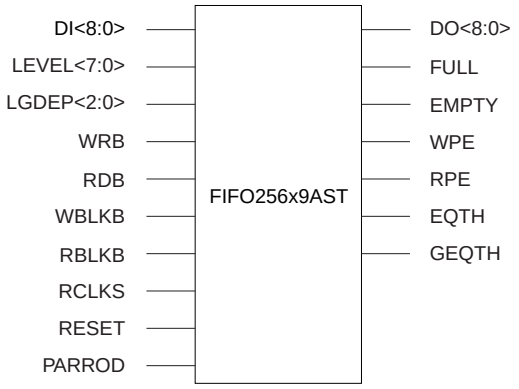
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9AST



Function

Asynchronous Write/Synchronous Read FIFO with Transparent Output and Parity Checking

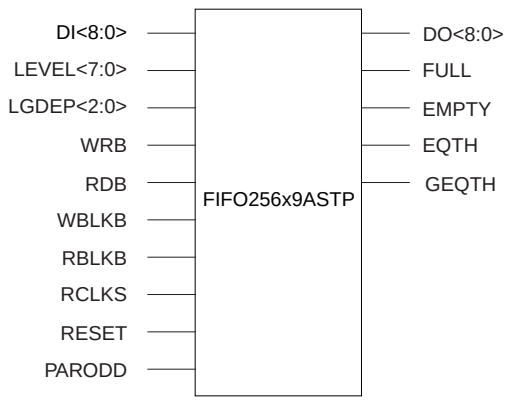
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9ASTP



Function

Asynchronous Write/Synchronous Read FIFO with Transparent Output and Parity Generation

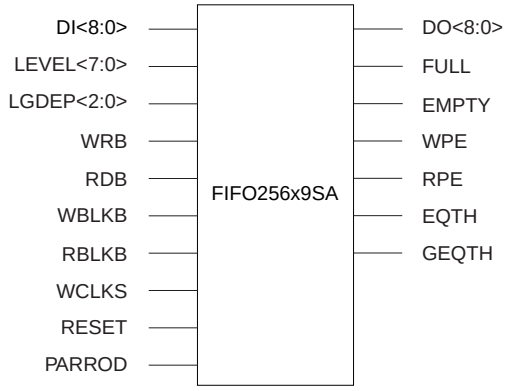
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SA



Function

Synchronous Write/Asynchronous Read FIFO with Parity Checking

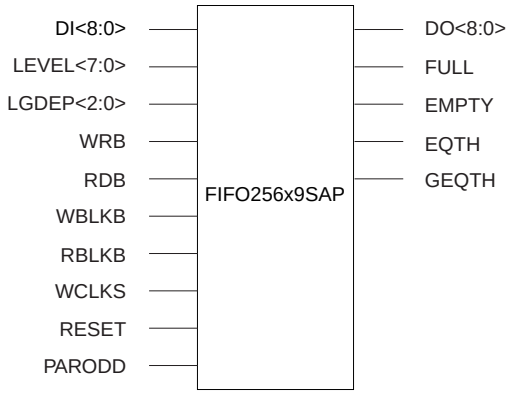
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SAP



Function

Synchronous Write/Asynchronous Read FIFO with Parity Generation

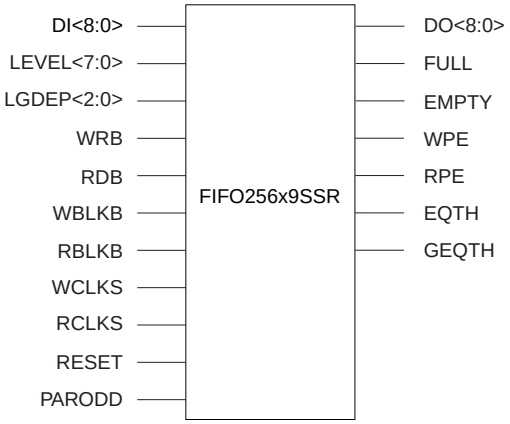
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SSR



Function

Synchronous Write/Synchronous Read FIFO with Registered Output and Parity Checking

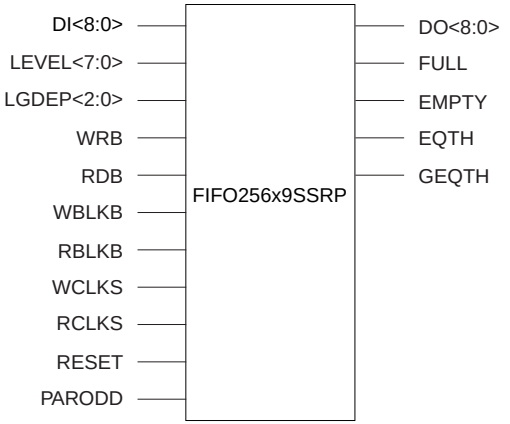
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SSRP



Function

Synchronous Write/Synchronous Read FIFO with Registered Output and Parity Generation

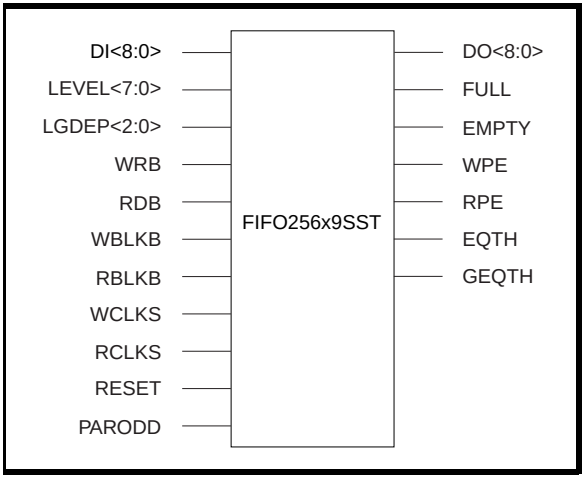
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

FIFO256x9SST



Function

Synchronous Write/Synchronous Read FIFO with Transparent Output and Parity Checking

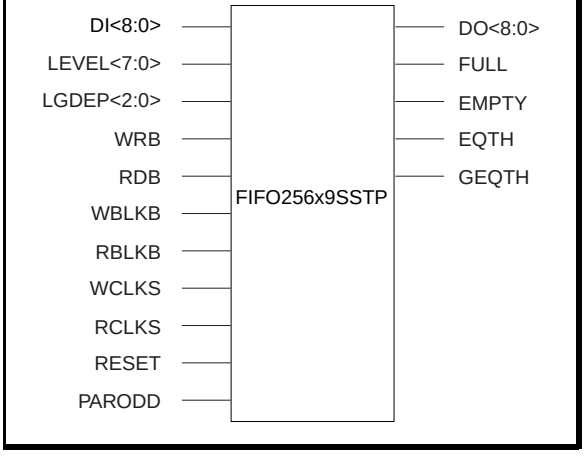
Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, WPE, RPE, EQTH, GEQTH

FIFO256x9SSTP



Function

Synchronous Write/Synchronous Read FIFO with Transparent Output and Parity Generation

Input

DI, LEVEL, LGDEP, WRB, RDB, WBLKB, RBLKB, WCLKS, RCLKS, RESET, PARROD

Output

DO, FULL, EMPTY, EQTH, GEQTH

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1256 305600.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is **tech@actel.com**.

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