Comparing FPGA Solutions

The key to comparing FPGA solutions is to highlight all issues that can significantly impact your end product and compare how each FPGA vendor addresses these concerns. The next task is to determine the relative value of each issue and then make an informed decision regarding your programmable solution.

Issues

Issues that can impact your products include the following:

- Schedule
- Product requirements (performance, area, cost, etc.)
- Compatibility with existing tool flows

Each of these issues is key to being able to deliver competitive products in a timely manner.

Schedule (Time to Market)

If time to market is a major concern for product success, then the FPGA should fit into this requirement as well. Some of the following are keys to ensuring that the FPGA is not the bottleneck in the design process:

- Performance and capacity must be predictable. When a design is partitioned (block diagram), the various functions and performance requirements are defined for each block. Ensuring that each block can achieve these goals prior to implementation is one key for controlling a schedule. Failure to meet a goal can cause severe schedule slips, forcing design modifications and potential vendor changes.
- The vendor must support fully automatic layout (place and route) that achieves performance and capacity expectations.
- Circuit boards must be built prior to FPGA completion to minimize schedule time. (This requires manual definition of I/O locations for the FPGA.) In many FPGA architectures, manual I/O assignment can significantly impact the performance and capacity of a device; therefore, you should verify with your FPGA vendor that this strategy will have little or no impact on your capacity and performance.
- Implementation and timing verification can represent a major portion of the design process. The FPGA vendor must have the tools and macros to move quickly through this process.

Note: *Actel has always delivered automatic layout tools that provide predictable performance and capacity by leveraging the strengths of its device architecture. The flexibility of the architecture also makes it possible to assign pins manually prior to device completion with minimal impact on performance or capacity and to prevent the printed circuit board from being the schedule-limiting factor. Actel also provides an array of implementation assistants including libraries (synthesis and schematic), ACTgen Macro Builder, and ACTmap VHDL Synthesis to speed users through the function-generation period of development. Actel also provides a variety of prelayout and postlayout tools to verify performance and to debug potential timing problems quickly.*

Product Requirements

Product requirements are the basic definition of an end product. The definition may include a variety of requirements such as cost, performance, area, function, I/Os, power consumption, etc. Meeting each of these goals can be critical for the success of your products. The following breaks down some of these attributes and provide information you should have to make an informed decision regarding your FPGA solution.

Performance

If performance is the primary goal, the following approach can be used to evaluate potential solutions.

1. Determine the performance of each major function in the design. It's a good idea to track capacity information as well, since high capacity can significantly impact the performance of many FPGA architectures.
2. Perform a critical path analysis to determine whether required performance is met. If performance is not met, then speed-graded versions or optional design implementations should be considered. Remember to consider both internal and external (I/O) performance.
3. Determine from the FPGA supplier whether the functions can be effectively mapped into the silicon at your performance and capacity expectations.

Note: *Again, Actel's goal is to provide complete cost/performance information to assist in making informed decisions. Capacity information for all functions is provided in terms of C-modules and S-modules, making it easy to track capacity. Performance numbers are provided in terms of both logic module delay and average routing delay so that there are no surprises. In fact, the defined delays represent average achievable performance from the automatic layout tools, providing performance margin for most designs, even at full device capacity. See individual data sheets for performance information on simple functions and the "Macro Libraries" section of the data book for information on more complex functions.*

Area

Another important factor driving the move to ASICs and FPGAs has been the ever-decreasing size requirements for products. This is especially true in the portable applications market. If minimizing board area is an important concern, then consider the following:

- Reduce package count when possible.
- Use smaller outline packaging when possible, such as TQFP and VQFP packaging.
- Use the smallest package that still meets minimum I/O count requirements.

Note: *Actel's antifuse-based devices provide single chip solutions with no requirement for external boot (including a ROM) circuitry. Actel also supports a wide variety of TQFP and VQFP packaging to meet small outline needs. In addition, the small die size of Actel FPGAs allows us to package high-capacity devices in small packages for applications that are gate limited instead of I/O limited.*

Cost

Cost can be one of the most difficult attributes to quantify when comparing multiple FPGA vendors. The main reason is that no effective standards exist in the industry for defining device capacity or performance. Each vendor has a unique architecture that is better for some functions than for others, and each vendor defines performance of devices uniquely. Performance and cost are closely coupled. Faster speed grade versions exist, but with higher price tags. So, if cost is a primary concern, then the following steps should be followed:

1. For each major function, estimate the number of resources required and the performance of each function for each vendor of interest.
2. Perform a critical path analysis to determine whether required performance is met. If performance is not met, then speed-graded versions, optional design implementations, or relaxation of performance requirements should be considered. Remember to consider both internal and external (I/O) performance in the analysis.
3. Determine the smallest device that accommodates the major functions, and ensure that it fits cost goals. (You may want to build in some overhead for unexpected changes and additions.)
4. Determine from the FPGA supplier whether the functions can be effectively mapped into the silicon at your capacity and performance expectations.

Note: *One of Actel's goals is to provide complete cost/performance information to assist in making informed decisions. Capacity information for all functions is provided in terms of C-modules and S-modules, making it easy to determine the required device size. In addition, all AC performance numbers are provided in terms of both logic module delay and average routing delay so that there are no surprises. See individual data sheets for simple functions and the "Macro Libraries" section of the data book for information on more complex functions. The architecture supports up to 100 percent usability of all resources in the device through automatic layout by leveraging architectural strengths.*

Tool Compatibility

Companies develop specific design flows based on specific CAE vendors to solve problems that are critical to their success. In order to be an effective hardware solution, FPGA development should also fit into this overall design flow strategy.

Note: *Actel FPGA development is based on interaction with third-party CAE tools. Actel's goal is to provide value-added functions over and above CAE tools while supporting the basic needs that designers face in developing FPGAs. See the "Software Development Systems" section of the data book for additional details.*