

Using Silicon Explorer to Debug the 100 Mbit Ethernet Dual-Port Bridge

The 100 Mbit Ethernet standard allows 10 Mbit Ethernet users to derive 10 times the performance from their wiring at little added cost. A dual-port bridge is described, consisting of SRAM, physical layer transceivers, and two Media Access Controllers (MACs). The MACs are implemented on a single Actel A1280XL FPGA (field programmable gate array).

This note describes a working 100 Mbit/10 Mbit Ethernet bridge using Actel A1280XL FPGAs. Several techniques were used during the design, test, and debugging of the design, which could be applied to a variety of design problems.

During the debugging cycle of the bridge design, the on-chip probe facility of the Actel A1280XL was used to help identify design errors quickly and easily. The on-chip probe allows the user to observe the state of any internal node on the chip in real time. The Silicon Explorer debugging kit facilitates the use of the on-chip probe with a powerful PC-based user interface. This application note will first review the design requirements of the 100 Mbit bridge and then describe the ways in which the probe facility helped accelerate the debugging cycle, reducing it to one five-day period.

System Architecture

The bridge system architecture is shown in Figure 1. It consists of the MAC, packet buffer storage (SRAM), and the physical interface devices. All MAC architectural blocks are contained in the FPGA. The system uses packet store-and-forward with a 16K x 64K SRAM for the buffer.

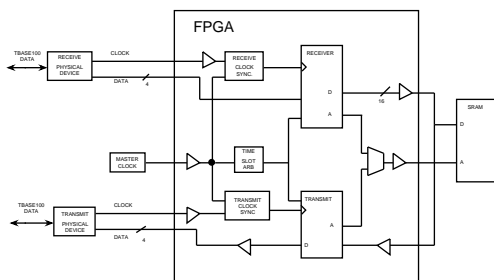


Figure 1 • Bridge System Architecture

All transfers between the MAC and physical level devices are nibble wide. Data between the memory and physical layer devices are concatenated or serialized by nibbles within the MAC.

The system has both a 25 MHz mode of operation (for 100 Mbit transfers) and a 2.5 MHz mode for the standard Ethernet data rate. The mode is determined by the clock as driven for the physical device.

Translation of data from the digital representation in the MAC to the physical level is performed by the physical-level device. The translation includes extraction/insertion of the 125 MHz transceiver clock, nibble encoding/decoding, and data-stream randomization.

Operation

Data traffic is half-duplex. The arbitration flip-flop divides the master clock into alternate 40 ns transmit and receive cycles. Separate transmit (TCLK) and receive (RCLK) clocks are derived from the master clock, which clocks the arbitration logic.

Four clocks are required for nibble-word conversion, each channel requires only one of the four clocks for a memory access. In normal operation, transmit and receive cycles are interleaved, as shown in Figure 2.

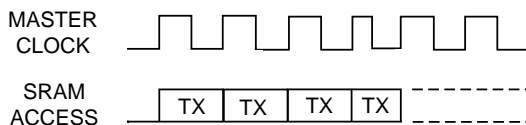


Figure 2 • Time Slot Arbitration

Receiving Data

MAC flip-flops synchronize receive requests from the physical layer device with the RCLK. When a request is received, it must be qualified by the arbitrator for a receive time slot. When qualification has been done, the address multiplex select lines are set so as to drive the receive address to the memory. Data words are written to memory.

Transmitting Data

Packets to be forwarded are read from memory as words, buffered, and multiplexed to the physical layer device as nibbles. Each complete word transmission causes the transmit address counter to be incremented for the next word read until the end of the packet.

Packet Maintenance

Packets whose addresses are in the range on the receive side of the switch are considered received and are discarded. Packets whose addresses are not on the receive side are forwarded.

In the simplex system described here, only two statistics are kept on packets—age and learn. *Age* refers to how recently the source address for a packet has been heard from on the network. If that time exceeds several minutes, the bridge assumes the source device is no longer active and will not maintain its address in the filter database.

The *learn* function is simply a table of known source addresses. Incoming packet addresses are compared with the contents of the learn memory space, and new addresses are added to it.

Design Techniques

Five days were required for debugging with one device programmed each day. The two debugging tools incorporated into the Actel ALS development system are the timing analyzer (Timer) and the probe. The Timer performs static timing analysis among any number of paths within the design, with stops at I/Os and flip-flop data inputs.

The Timer was used to analyze the clock path delays. Clock skew and synchronization issues frequently arise in multiple clock applications, such as data-communication systems. The Timer provided feedback through the iterations of the design to isolate and solve the problems described here.

Meeting the clock tree requirements for the design proved to be the most difficult design challenge. With the transmit and receive logic each requiring about 45% of all the flip-flops in the design and the arbitration using the remaining 10%, an effort was required to minimize skew between the clocks. All clocks had to have a skew of no more than ± 5 ns. Each of the two ACT 2 dedicated clock lines was used for the transmit and receive functions. As a result, ordinary routing resources were used for the arbitration clock. Use of such resources required skew compensation, as shown in Figure 3.

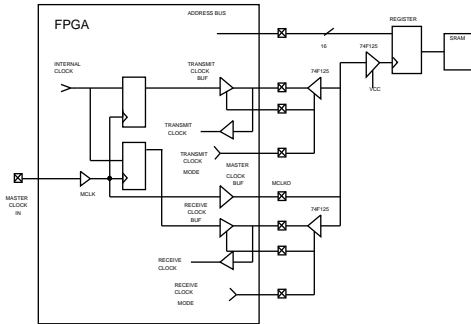


Figure 3 • Clocking with Delay Compensation

Clocking Delay Compensation

The FPGA has to be able to operate in two modes, 10 Mbit and 100 Mbit, simultaneously, since either the transmit or receive side can be in either mode. The slower speed clock is generated internally; the faster clock is driven from an off-chip 74F125 three-state buffer. The mode selects either the fast or slow clock dynamically. Mode information comes from the physical layer devices.

It is important that the 25 MHz and 2.5 MHz clocks be closely synchronized, because memory transfers must occur on the same clock boundary to avoid conflict. Synchronization is achieved by matching the delays of both the clock paths. As shown in Figure 3, the master clock (MCLK) from the physical devices is synchronized with the internal 2.5 MHz clock by using two flip-flops. The flip-flops drive the outgoing paths of bidirectional I/O buffers. Each bidirectional buffer pad is also driven by a 74F125 three-state buffer whose source is the master clock.

The master clock output delay matches the delay through the output of the bidirectional buffers, and they cancel each other. The 74F125 TTL buffer and the delay from the internal flip-flop both have 5 ns delays and cancel out each other. Matching the delays of the two clock paths allows either channel to use either clock and have them completely synchronized.

Memory Interface Design

Another issue pertains to the latency required to drive addresses to the memory. About 60 ns are required from the time MCLK is applied to the pad until a valid address is driven off the FPGA. Since the master clock period is only 40 ns, the delay in generating an address, without some kind of compensation, would be too great. Part of the solution is to use an external pipeline register to allow a full 40 ns of address delay

by having the memory access occur during the next clock. The register also provides greater drive strength to the memory inputs by reducing noise from simultaneously switching outputs. Still, the address must be valid when it reaches the register inputs.

Further timing compensation is performed by balancing the address delay with other delays. The delay from the master clock input pad to the master clock output pad is 18 ns. The clock then goes through a 74F125 buffer, adding another 5 ns delay. The total delay, 23 ns, subtracts from the address delay, because both begin from the same pad. The effective delay for the address is only 37 ns, well within the requirement.

Silicon Explorer

The typical design cycle for FPGAs starts by first completing FPGA compilation and place-and-route, and it continues with FPGA debugging, which includes programming the prototype FPGA and performing diagnostics on the design. This procedure is repeated until the design has been debugged. To do these tasks, designers need constantly to move and transfer design information back and forth from their PCs to the board and to the lab. Comprehensive verification of an FPGA in real time and on the board is practically impossible. To perform a real time debugging of the design, designers must respin the design to isolate internal nodes in question through external pins so that they are observable using a logic analyzer or an oscilloscope.

What is Silicon Explorer?

Silicon Explorer is a debugging and diagnostic kit available to Actel designers. It combines the embedded internal probing features of Actel devices with an integrated PC-hosted logic analyzer window to equip designers using Actel will all they need to prototype and debug their designs, using only their PCs. This embedded probing feature allows designers to view the activities of each internal node of the FPGA in real time, while operating in their systems. This powerful feature makes it extremely easy to locate design defects quickly.

Silicon Explorer features include the following:

- Real-time access to selected internal nodes
- No required changes in design
- Tight integration with PC-hosted logic analyzer
- Control directly from a PC
- Serial port connection
- 18 channels
- Up to 100 MHz sampling
- User-friendly software for viewing and analysis

The Silicon Explorer kit, shown in Figure 4, includes the hardware and a logic analyzer. The hardware peripheral connects to the serial port of your PC and acts as the interface between the PC and the FPGA on the board. The PC-hosted logic analyzer is an intuitive, easy-to-learn, and easy-to-use Windows-based analyzer with 18 channels sampling as high as 100MHz. Both the Silicon Explorer peripheral and the logic analyzer integrate with Actel's Designer Series FPGA development tools. Once the FPGA has been placed and routed, internal nodes in the FPGA can be selected for viewing and analysis.

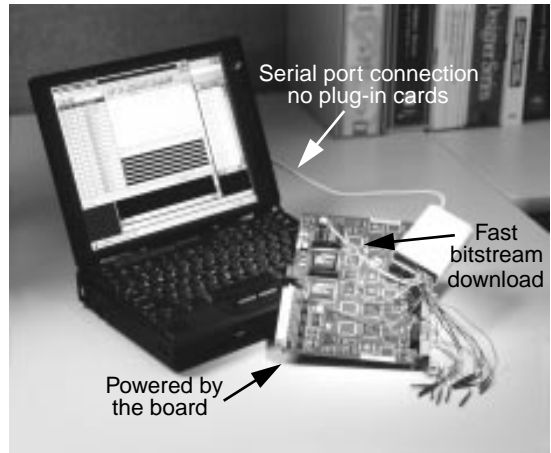


Figure 4 • Silicon Explorer Kit

Using the Silicon Explorer

For debugging purposes, the user will be able to select internal nodes from the Designer Series software. The programming and debugging software within Designer, Explorer Manager, has a user-friendly interface, which shows the internal module cells of the design (see Figure 5). Once the nodes are selected, they are accessible to the user through the external I/O pins or the PRA or PRB I/O pins. A logic analyzer connected to these pins can then be used to observe the internal operations of the device, eliminating the guesswork usually required when doing system debugging.

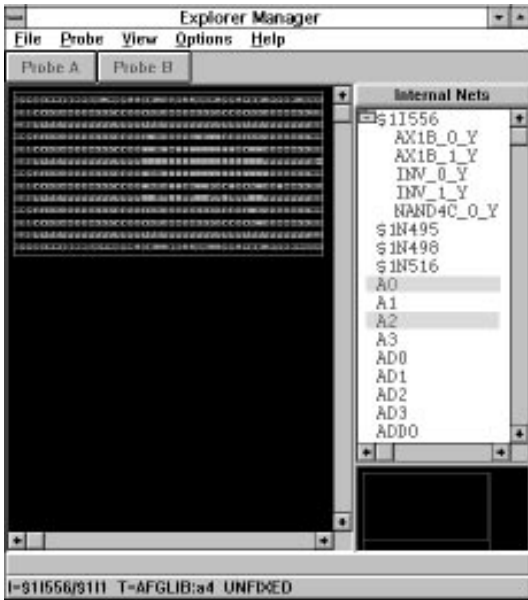


Figure 5 • Explorer Manager Window

Probe Debugging Techniques

For the synchronous portions of the design, verification was performed with backannotated simulation. Simulation, however, is not adequate to cover all the cases for the logic dealing with asynchronous events. That logic must be debugged in the system by using the in-circuit probe. The two probes are features of the Actel Designer Series development system. They are used to point inside the device to any two nodes at a time to see their logical state at full frequency.

One use for the probes in debugging the design is to examine, node by node, the events inside the device following a reset. When an error in the design prevents recovery from a reset, I/Os don't provide the information to understand what went wrong. The probe, used in conjunction with a reset pulse generator, unmask the problem.

Conclusion

Silicon Explorer is a key tool in speeding time to market for Actel-based FPGAs. This note demonstrates the use of Silicon Explorer during the debug portion of the design of a 100 Mbit Ethernet dual-port bridge.

Actel and the Actel logo are registered trademarks of Actel Corporation.
All other trademarks are the property of their owners.



Actel Corporation

955 East Arques Avenue

Sunnyvale, CA 94086

Tel: (408) 739-1010

Fax: (408) 739-1540

Actel Europe Ltd.

Daneshill House, Lutyens Close

Basingstoke, Hampshire RG24 8AG

United Kingdom

Tel: (+44) (1256) 305600

Fax: (+44) (1256) 355420