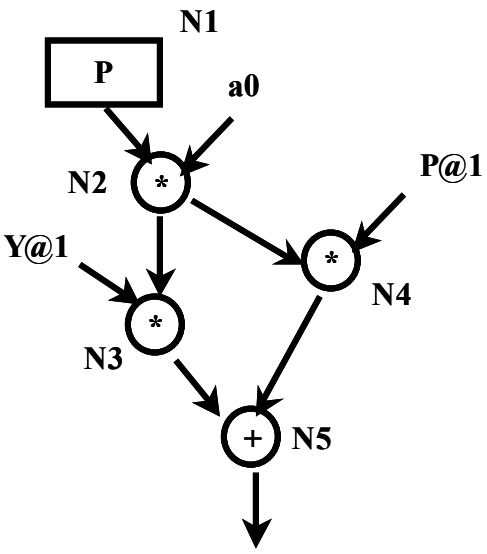
EE 4743 Test #2 Solutions – Spring 2003

For any partial credit, you must show your work. Problems 1-3 must be answered. You may skip TWO questions out of problems 4 through 14 (cross out the two questions that you DO NOT want graded). In all flowgraphs, chaining of execution units is not allowed.

1. (20 pts)

a. Assuming no overlapped computations, and no pipelined execution units, an no restrictions on the number of executions units or input busses, what is the minimum latency (in clock cycles) of the flowgraph at the right.? **4**

b. Using one multiplier, one adder, and on input bus, give a schedule for the flowgraph. You DO NOT have to show register allocation.

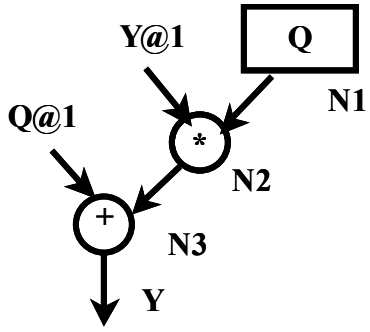


	Multiplier	Adder	Register transfer ops
Clk 1			**N1**
Clk 2	**N2**		
Clk 3	**N3 (or N4)**		
Clk 4	**N4 (or N2)**		
Clk 5		**N5**	
Clk 6			

2. (20 pts)

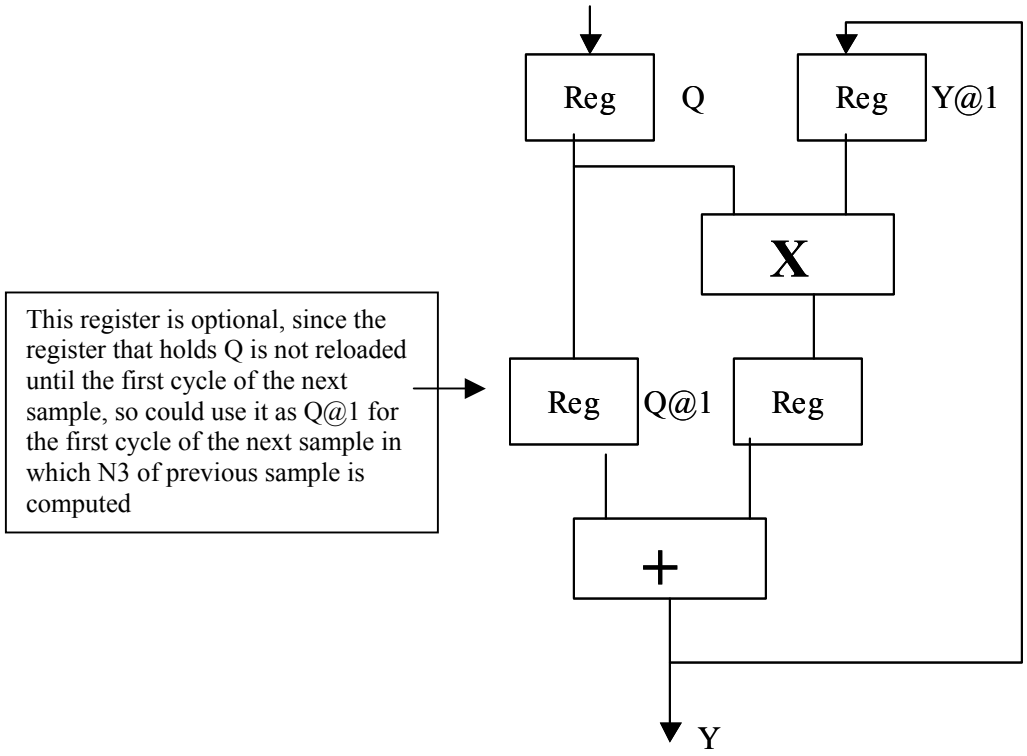
a. For the flowgraph at the right, show schedule with latency of 3 clocks, and initiation period (rate) of 2 clocks. You can use any number of input busses

b. Draw the datapath for your schedule. Show everything except the FSM.



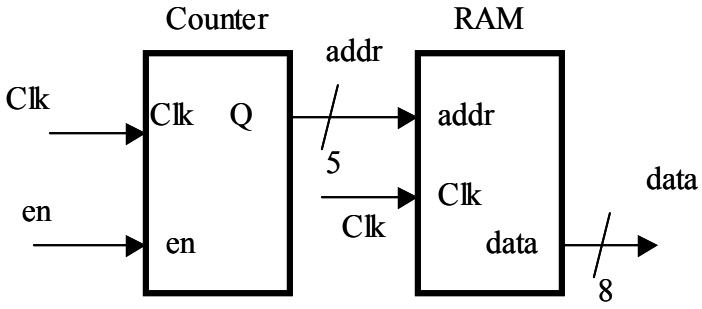
	Sample J	Sample J+1	Sample J+2	Sample J+3	Sample J+4
Clk 1	**N1**				
Clk 2	**N2**				
Clk 3	**N3**	**N1**			
Clk 4		**N2**			
Clk 5		**N3**	**N1**		
Clk 6			**N2**		
Clk 7			N3		
Clk 8					
Clk 9					
Clk 10					
Clk 11					
Clk 12					
Clk 13					
Clk 14					

Datapath for problem #2.



3. (15 pts)

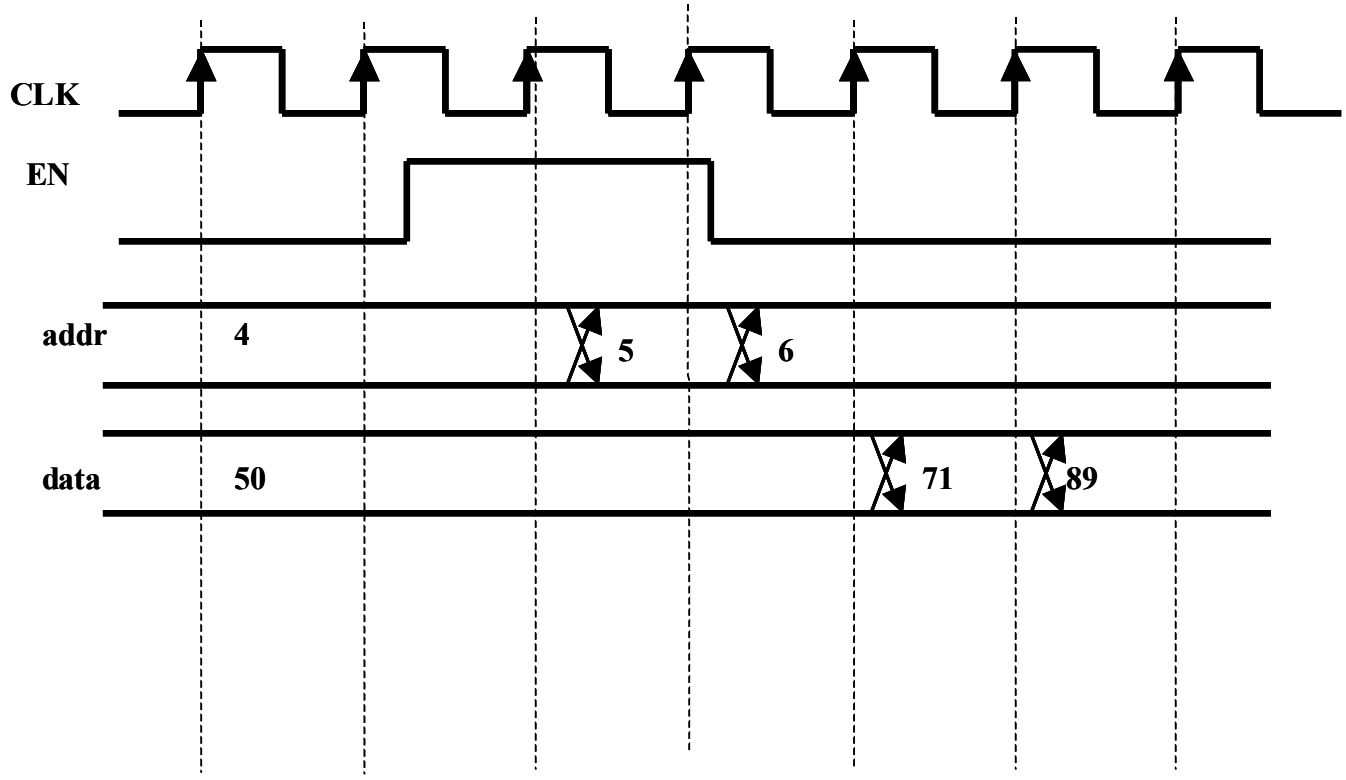
Fill in the timing diagram below for the counter/ram combination shown on the right.



RAM addr/control is registered, data is also registered.

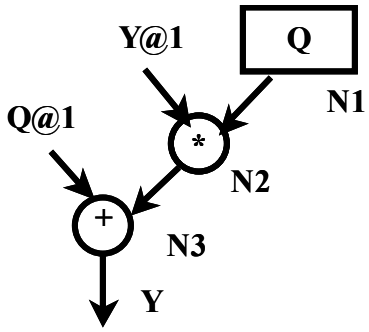
The counter is an UP counter.

RAM locations contain: loc 4 = 50, loc 5 = 71, Loc 6 = 89, Loc 7= 95, Loc 8 = 22



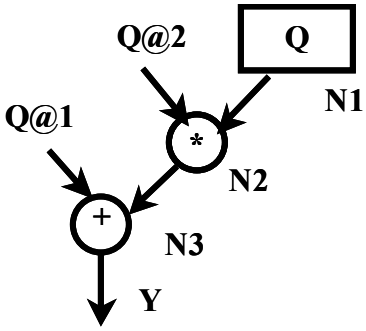
4. (5 pts) For the flow graph show below, if I pipeline the multiplier by one stage, what is the MINIMUM achievable initiation period (in clock cycles). A smaller initiation period means a faster initiation rate.

Minimum is 3 clocks because of N2, N3 dependence on previous output – N2 will take 2 clocks, N3 one clock.



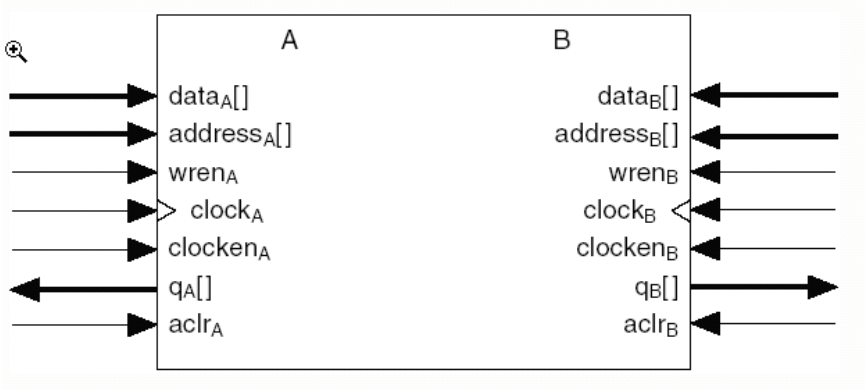
5. (5 pts) For the flow graph show below, if I pipeline the multiplier by one stage, what is the MINIMUM achievable initiation period (in clock cycles). A smaller initiation period means a faster initiation rate.

Minimum is initiation period of 1 clock – all computations can be fully overlapped because no dependence on previous output.



6. (5 pts) The picture below is an SRAM type supported in the Altera Stratix FPGA. What type of SRAM is this?

True dual-port SRAM



7. (5 pts) The Altera Stratix FPGA offers three different IO types: Single-Ended, Differential, Voltage-referenced. For each of the statements below, circle each type that applies (you can circle more than one).

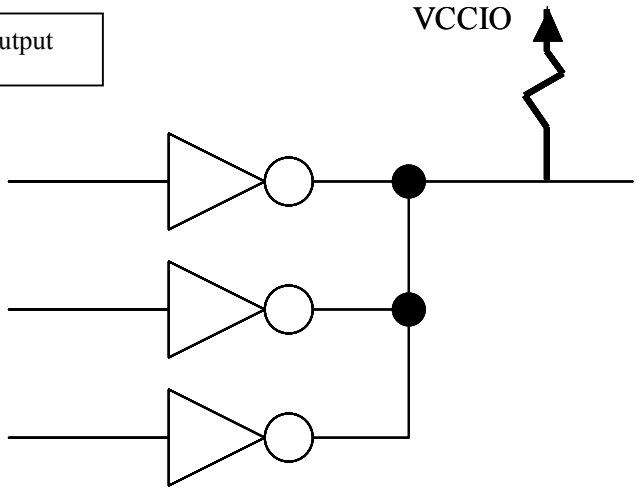
a. Rejects common-mode noise. Single-Ended **Differential** Voltage-Referenced

b. Limited swing signaling Single-Ended Differential **Voltage-Referenced**

c. Swings between 0 and VCCIO **Single-Ended** Differential Voltage-Referenced

8. (5 pts) If I wanted to implement the IO shown below, what output configuration option would I need to use in the Altera Statix IO cell?

Open drain output



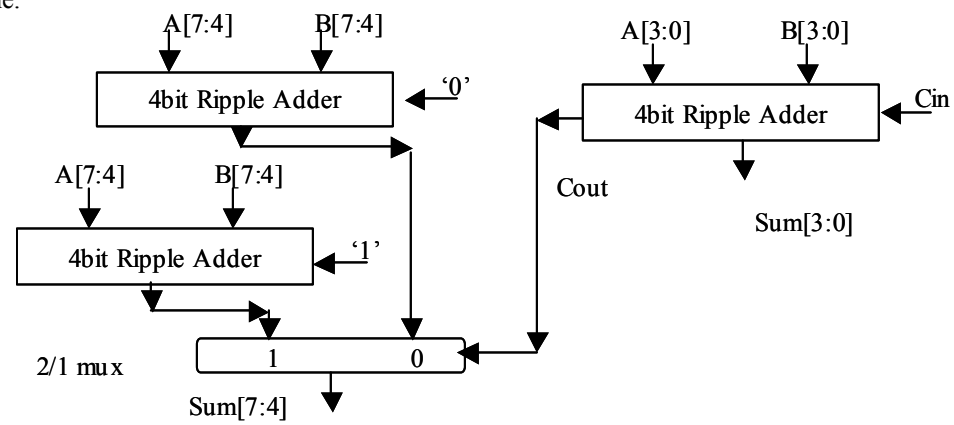
9. (5 pts) Assume that the magnitude of output voltage swing of the IO lines is fixed, there are two principle methods for reducing 'ground bounce' (voltage induced on the ground plane due to inrush current). Give these methods.

Inrush current due to L* di/dt
Reduce L by adding multiple Vdd/Gnd pins
Reduce di/dt by slowing down signal transitions (reduce slow rate).

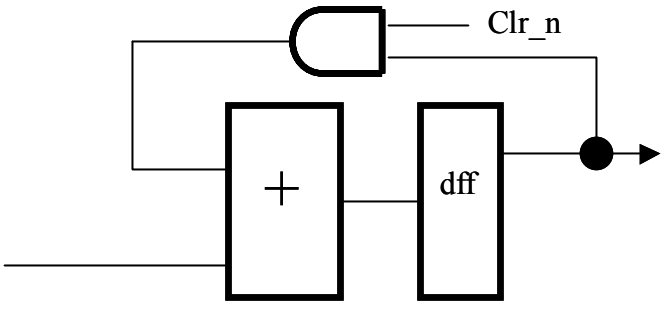
10. (5 pts) A hierarchical clock network was added in the Altera Statix FPGA – what was the principle reason for doing this?

Added to reduce maximum slew in regions of the device. Maximum clock skew on regional clocks less than maximum skew on global clocks.

11. (5 pts) Draw a quick sketch that clearly illustrates the speed advantage of a carry-select adder scheme.



12. (5 pts) The Altera Stratix FPGA included a monolithic adder in an 'accumulator' configuration. Draw a quick sketch that shows what an *accumulator configuration* means.



13. (5 pts) What are two methods for controlling signal corruption due to transmission line reflections?

Reduce slew rate to reduce signal rise/fall times (when signal time of flight is long compared to signal rise/fall time, reflections become a problem – make signal rise/fall times longer means that longer wires can be used before reflections become an issue)

Add termination resistors at signal endpoint.

14. (5 pts) Give two new features that were included in the Stratix basic Logic Element that were not present in the Altera Flex

XOR gate for more efficient implmentation of adder/subtractor
Generalized cascade chains for LUTs
Synchronous clear logic
Configuration options to LUT4 to support carry select adder functionality.