ASIC 120: Digital Systems and Standard-Cell ASIC Design

Term: **Fall 2005**
Lecture Room: **DWE 3516**
Instructor: **Jeff Wentworth,**
4B Computer Engineering,
j.wentworth@gmail.com
Course website: **www.asic.uwaterloo.ca (under the Resources tab)**

Course Summary:
These lectures will start by covering the basics of digital circuits, and will progress quickly through more advanced digital design, FPGAs, practical implementation and debugging techniques. The idea of these tutorials is not to go line by line through code, nor fill blackboards with lots of proofs and mathematical equations. Rather, we aim to provide a comprehensive grounding in digital systems design that goes above and beyond, but is complementary to, the fundamentals you will learn in courses like ECE 222, 223, 324, and 427.

Lecture slides will be posted to the website. Lectures will be recorded and available for download in MP3 format via iTunes (under the Educational section) or using your favorite RSS feed aggregator.

The tutorials are free, open to anyone who's interested, and there's no obligation to attend future tutorials. Invite your friends!

Course Outline:

LECTURE 1: INTRODUCTION TO DIGITAL CIRCUITS
When: Tue, Oct 11, 17:30 - 19:00
Where: DWE 3516
Summary:
- overview of combinational and sequential systems and why they're useful
- logic gates: NOT, AND, NAND, OR, NOR, XOR, XNOR
- basic combinational structures: mux, half adder, full adder
- sequential structures: flip flops and state machines
- HDLs and why they're useful

LECTURE 2: INTRODUCTION TO VHDL
When: Wed, Oct 19, 17:30 - 19:00
Where: DWE 3516
Summary:
- covering again most of what was taught in Tutorial 1, but relating it to VHDL
- the idea is to separate VHDL from traditional programming languages like C and Java by showing that the thought process involved in digital design is fundamentally different

The remaining tutorial topics are tentative and may be customized to the students demands.

LECTURE 3: INTERMEDIATE VHDL (Oct. 26)
- if-generate, for-generate
- VHDL 1992 vs. 2000 (or whatever - I can't remember the names of these two standards)
- splitting a VHDL project across multiple files
- test benches

LECTURE 4: DIGITAL SYSTEMS CONCEPTS (Nov. 9)
- the FPGA: LEs, buffers and routing, other resources
- bus interfaces
- register files
- FPGA hardware features in more detail: clocks, memories, memory interfaces
- soft- and hard-processors in FPGAs

LECTURE 5: PRACTICAL DIGITAL DESIGN (Nov. 22)
- software tools: Quartus, ISE, NC-VHDL (ideally, I will demonstrate them all, with focus on one of them)
- hardware tools: logic probe, oscilloscope, logic analyzer (not to be demonstrated, but discussed with pictures)
- putting these together in board-level digital design
- from VHDL to an ASIC

LECTURE 6: CASE STUDY - SENIOR COURSE CODE REVIEW (date TBA)
- here I will dissect a fourth year-type project in our, going over one solution (ours), and writing some code by committee

LECTURE 7: CASE STUDY- UW ASIC DIGITAL VIDEO PROCESSOR (date TBA)
- here I will dissect our own design, first through the use of high level diagrams, and then by delving into the code
- the idea is to introduce everyone to the work we've already done

Text Book:
None.

Reference Material:
Will be provided during the course.