A LOCAL TIME MANAGEMENT SYSTEM ASSP

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Abstract

Previously there have been difficulties in accurately establishing the time correlation between events reported on ground via packet telemetry data and their actual time of occurrence in an onboard application. The Local Time Management System is a radiation hard component enabling users to overcome this problem by time stamping data at source. The high resolution and precision of the local time reference, with which data may be time stamped, is maintained automatically by this new component.

1 INTRODUCTION

With the advent of packet telemetry, the time correlation between the generation of onboard data and its reception on ground has become more complex compared to previous use of fixed frame protocols. Packet telemetry allows dynamic bandwidth allocation schemes, buffering etc., making it flexible and adaptable. This however leads to an asynchronous delivery system which is no longer fully deterministic in that the sampling instant is not related to a position in the transfer frame. The task of determining the time when data were sampled or generated onboard is therefore not simple anymore. Hence, new methods are required for providing the users with time information related to the telemetry data stream.

The purpose of the Local Time Management System (LTMS) component is to provide time coherence throughout the spacecraft without requiring processing power from the applications using it. It provides a time stamp facility for datation of events, an alarm clock, a pulse generator, a waveform generator and a stopwatch.

The LTMS is being developed by IMEC (B) under the prime contractor Dornier Satellitensysteme (D) and will be manufactured by MITEL Semiconductors (S) in their radiation hard SOS5 process. The capability assessment programme for the SOS5 process will be completed in 2Q97 and it is expected to receive ESA Capability Approval in 2Q98. The foundry (former ABB Hafo) will support the LTMS as an Application Specific Standard Product (ASSP), with a complete data sheet (Ref. 1). First prototypes are expected in 2Q97.

The development is funded by the European Space Agency and is managed by the Microelectronics and Technology section at the European Space Research and Technology Centre.

The concept of decentralised onboard time references is discussed in the next section, followed by a description of how time coherence is achieved with the LTMS and what kind of time facilities it offers. An example of how the LTMS can be used together with the On-Board Data Handling (OBDH) bus is provided. Finally, the design methodology applied during the development of the LTMS component is presented.

2 DECENTRALISED ONBOARD TIME DISTRIBUTION

The general approach to accurately maintain onboard time is to have a central time reference measuring the elapsed time from an arbitrary epoch and to distribute regularly this time information to onboard applications by means of messages and synchronisation pulses. Each application maintains its local reference of the elapsed time which it synchronises with the central time reference using the aforementioned means.

Another approach would be to have a centralised time system, where each application that needs to time stamp data could request the unit maintaining the central time reference to provide the relevant time information. Such an approach would have several inherent drawbacks, e.g. in systems with many users, the accuracy of a time stamp could be jeopardised due to long service latency and excessive bus traffic could degrade the overall performance of the OBDH system. These reasons have made the distributed approach the preferred one and it has been selected for a standard that will govern the time distribution on future spacecraft.

Previous implementations have required support from the application processor to maintain synchronisation between the central and the local time references. Protocols and formats for distributing time information have differed between spacecraft and have sometimes only provided low resolution or poor accuracy.

The purpose of the LTMS is to provide an accurate time coherence throughout the spacecraft without requiring any processing power from the applications using it. The LTMS does not only provide local time information to its users, but also implements advanced checks in order to determine the quality and validity of the received time information. This point has very often been neglected in past implementations where the loop was left open, e.g. users were not warned when faulty time information had been received due to transmission errors, synchronisation problems or other error sources.

The LTMS implements the incoming ESA standard specifying a time distribution protocol as shown in figure 1. This makes the component suitable for use on future spacecraft. The protocol has been defined in a way that

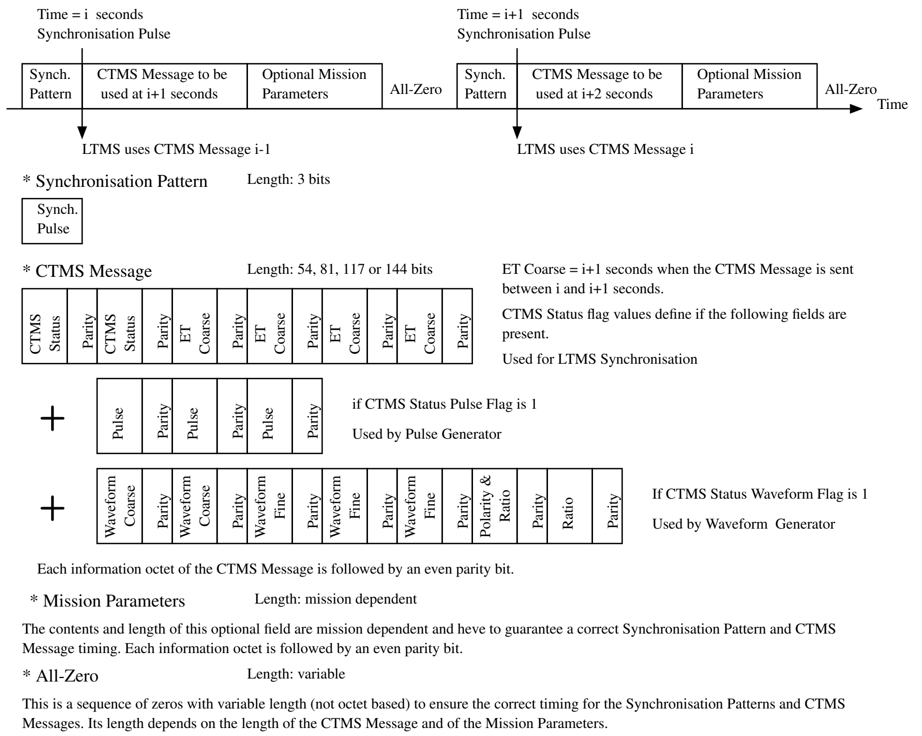

Figure 1: *Serial message format and synchronisation pulse timing*

exploits the synchronous distribution capabilities of the OBDH bus to eliminate any requirements for additional harness or dedicated interrogation/response traffic, although being suitable for other types of data buses as well. The protocol does not disrupt other users (in different terminals) in case one user is out of synchronism. By contrast, e.g. in the ERS spacecraft, all users have to be disrupted in case a single local time counter fails.

The correlation between the central time reference and ground has already been foreseen by providing a time strobe from the Virtual Channel Assembler (VCA) component situated in the telemetry encoder (also manufactured by MITEL Semiconductors). The VCA time strobe has a deterministic relationship to the bit structure of the telemetry frame. This makes it possible to establish the time relation between the assertion of this time strobe onboard and the reception of the relevant frame on ground, taking into account the down link propagation delay. This involves sampling the central time reference at the assertion of the time strobe and sending down the value in a telemetry packet. The relation between the elapsed onboard time and the local time of the receiving ground station can then be determined.

As will be explained, each LTMS maintains its own phase locked copy of the central elapsed time reference with which onboard applications can time stamp their data. This unbroken chain of time relationships onboard, and between the spacecraft and ground, provides a solution to the problem of knowing when an event took place onboard a spacecraft in any given space-time frame.

3 TIME COHERENCE WITH THE LTMS

The LTMS maintains a local copy of the central elapsed time (ET) reference and is typically embedded in the host application. The format of the ET is shown in figure 2. All time information sent to or provided by the LTMS is compliant to the CUC format described in the CCSDS Time Code Standards (Ref. 2). The LTMS ET counter is the local time reference consisting of the fine ET counter (22 bits with sub-second weights) and the coarse ET counter (32 bits, with the least significant bit having a weight of 1 second). The full ET counter provides a wrap-around period of 136 years, which should be more than sufficient. The ET counter resolution depends on the selected operating mode of the LTMS. As a result of this, the least significant bit of the ET counter can have the weights 2^{-22}, 2^{-21}, 2^{-20} or 2^{-19} of a second, corresponding to a resolution between approximately 240 ns to 2 µs.

The central ET reference is assumed to be managed by the Central Time Management System (CTMS). Coherence between the central and the local ET references is maintained by means of synchronisation information distributed from the CTMS. The LTMS performs regular synchronisations with respect to the central ET reference using this information. The information provided by the CTMS to the LTMS comprises messages containing time codes, synchronisation pulses and phase references.

Every second a message including a time code is broadcast from the CTMS to all LTMS components in the system. Each message is followed by a synchronisation pulse which

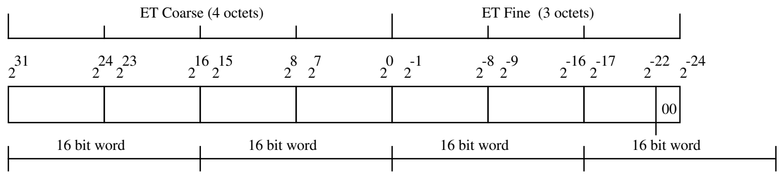

Figure 2: *LTMS elapsed time format*

acts as a `mark' to establish the instant at which the delivered time code is applied. The synchronisation pulses occur at one second intervals and coincide with the increments of the units of seconds bit in the ET counter. No sub-second information needs to be included in messages sent by the CTMS.

The messages accepted by the LTMS are compliant with the Serial Time Distribution Protocol as defined by the 4-255 Data Bus Protocol Extensions (Ref. 3). These messages can be acquired through a bit serial interface or via a parallel microprocessor interface. In the serial protocol, as has been depicted in figure 1, the messages are Manchester encoded and also carry the synchronisation pulses and phase references. To get the best accuracy, this information should be delivered by a system which is coherent with the clock of the central time counter.

The parallel protocol, not shown here, is similar to the serial one, but does not include parity or optional mission parameters. The parallel interface is compatible with the ERC32 and MA31750 (both Mark-I and Mark-II) microprocessors, requiring little or no additional external hardware for connecting them together. The input clock driving the microprocessor interface is decoupled from the rest of the LTMS allowing the microprocessor to operate at an arbitrary frequency.

The LTMS checks the format and contents of the received messages and also the timing of the synchronisation pulses. If all this is found to be correct, a re-synchronisation of the LTMS ET counter is performed on the detection of the synchronisation pulse when required. This synchronisation consists of loading the received time code into the coarse part of the ET counter and resetting the fine part of the ET counter to zero. The size of the time window in which this synchronisation instant is allowed to occur is configurable. Monotonic ET count with resolutions down to 2^{-20} of a second can be maintained, corresponding to approximately 1 µs. Note the difference between the synchronisation process in the LTMS and previous implementations: no time discontinuities need to occur in the LTMS ET counter.

When errors are detected in messages or in the timing of the synchronisation, the built-in error handling will limit the consequences thereof not to unnecessarily upset the local ET. A dedicated output pin continuously informs about time validity. The time validity of the ET counter and the overall results of the internal error checkers related to the synchronisation process can also be monitored by reading a status register.

The CTMS provides the LTMS with phase references to which the clock driving the ET counter can be adjusted. The clock driving the LTMS ET counter does not need to originate from the CTMS and may thus be generated locally. This clock may be provided from external circuitry, e.g. the OBDH bus clock, and should then be consistent with the desired ET resolution and be acting as the phase reference. Alternatively, the LTMS may derive it from a supplied 224 Hz (≈16.77 MHz) crystal or clock signal. The built-in crystal oscillator requires only a crystal, two capacitors and a resistor to operate, and can also be used for driving external components such as a microprocessor. The internally derived clock can be slaved to the incoming phase references by either using the built-in or an external Digital Phase Locked Loop (DPLL).

When the LTMS is operated with such a derived clock, the phase references do not have to occur at regular intervals since the use of a DPLL offers a free-wheeling capability in case of phase reference drop out. Note that this also enables the LTMS to maintain an ET counter with a higher resolution than the provided phase references. In case of requiring maximum resolution coupled with infrequent phase references, an external DPLL would have to be employed if crystal stability does not meet the requirements posed by the built-in DPLL. The LTMS phase reference frequency is configurable to match various types of surrounding equipment, such as the OBDH and the Mil-1553B buses.

The LTMS can also operate in stand alone mode without a central time reference. It then maintains its own time reference and no synchronisation is required. It is however possible to initialise the LTMS from time to time via the parallel microprocessor interface. This provides the capability to use the LTMS even when no CTMS is available in the system, making it backward compatible with some earlier equipment.

4 THE LTMS TIME FACILITIES

The LTMS provides its users with more than just a high quality local time reference. It provides time facilities that are accessible via the parallel microprocessor interface as can be seen in the LTMS block diagram in figure 3. They can be controlled and observed via dedicated inputs/outputs as well as via control registers.

The Time Stamp facility allows the LTMS user to time stamp data. An external event on a dedicated time strobe input is used to latch the ET counter value into a facility

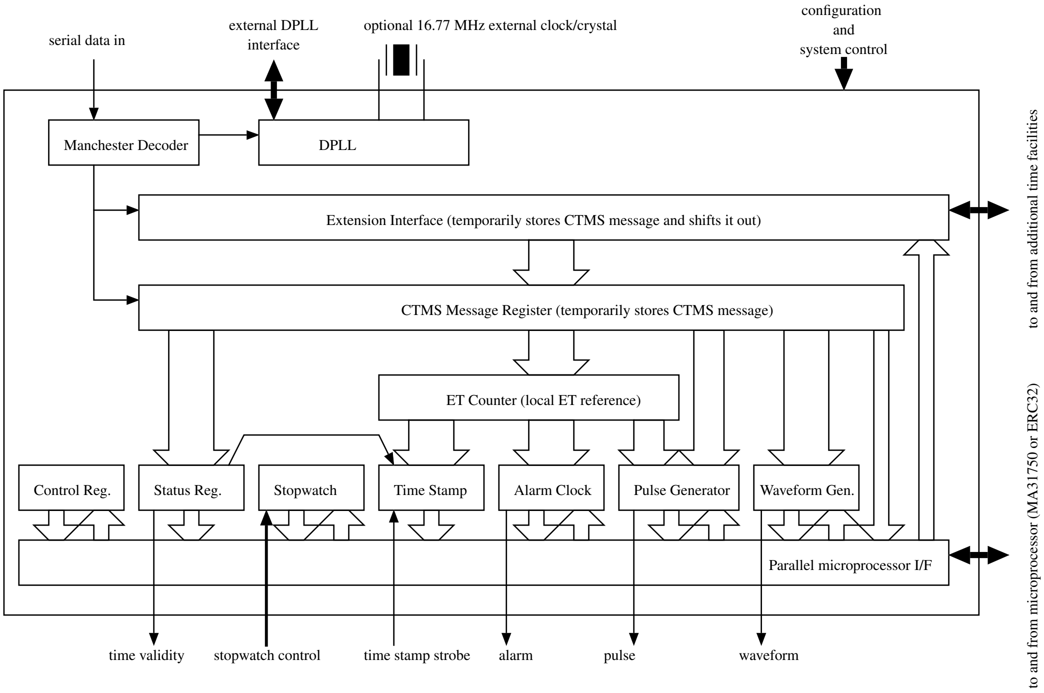

Figure 3: *LTMS block diagram*

register. Additionally, the status of the LTMS and the rest of the time distribution chain is latched on the event. The register contents can then be read via the microprocessor interface and associated with the corresponding data. A time strobe event can also be induced by writing to a control register. Events on the time strobe that occur before the registers have been fully read after a previous event are flagged in a status register, providing the users with information about the validity of the datation. The time resolution of this service is the same as for the ET counter.

The Alarm Clock allows the LTMS user to generate an alarm occurring at desired ET values, programmed via the parallel microprocessor interface. The alarm will be set off immediately if a time that already has been past is written, thus preventing potential system deadlocks. At the alarm time, a dedicated output pin is asserted and stays so until a new alarm time has been programmed. The time resolution of this service is also the same as for the ET counter.

The Pulse Generator facility enables the CTMS to generate pulses on a LTMS output pin at a maximum rate of 1 Hz. The pulses are controlled by the phase field in the CTMS message and are generated at the instant the monotonic field of the LTMS counter becomes equal to the supplied time information. A prerequisite for generating a pulse is that the corresponding CTMS message has been qualified and used for the synchronisation of the LTMS ET counter. Consequently pulses are generated in phase with the central time reference.

The Waveform Generator facility allows the CTMS or the LTMS user to generate a periodic pattern on a dedicated LTMS output pin. The pattern period and duty cycle are programmable via the waveform field in the CTMS message or via the parallel microprocessor interface. The time resolution for this generator is the same as for the ET counter.

The pulse- and waveform generator facilities can be combined to form a programmable frequency generator by simply connecting some LTMS pins to each other. This combined generator can create periodic and phase controlled patterns and is under the control of the CTMS.

The Stopwatch facility allows the LTMS user to measure elapsed time between events with a resolution down to 2^{-24} of a second, corresponding to approximately 60 ns. It can also count the number of events within a predefined interval. The intervals can be as long as 18 hours and approximately a billion events can be counted. These measurements are unaffected by the LTMS synchronisation process. A measurement can be suspended and continued at any time. The end of a measurement or saturation of a counter are flagged in a status register, providing information regarding the validity of the measurement.

With its extension interface the LTMS enables board designers to extend or customise the on-chip time facilities with a minimum of external hardware. All information fields of the CTMS message are serially shifted out via this interface. The LTMS component relieves its host system from any processing load associated with the provision of ET at local level when implementing external time facilities.

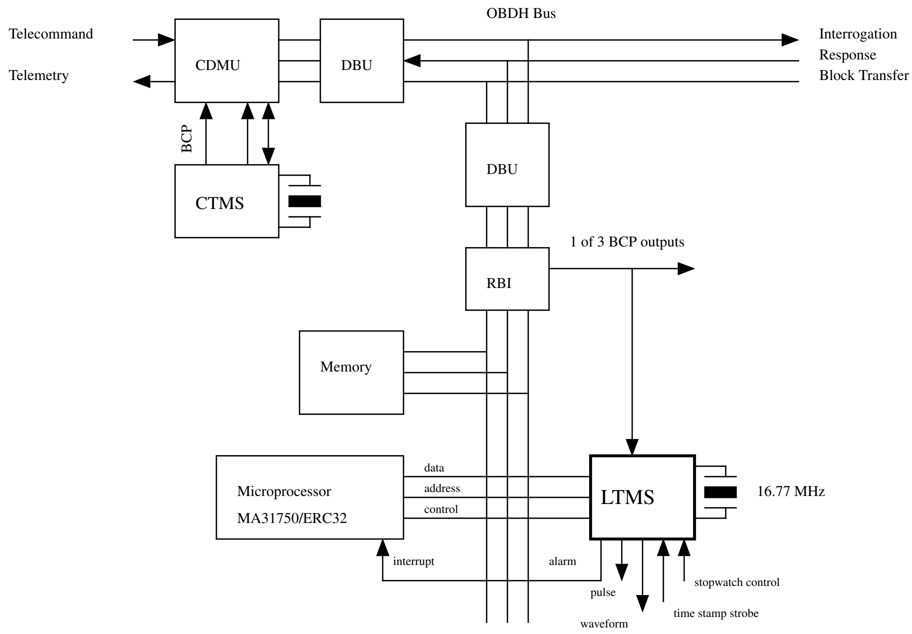

Figure 4: *The LTMS in a typical OBDH system configuration*

5 USING THE LTMS IN AN OBDH APPLICATION

Most LTMS applications are expected to involve the OBDH bus. Figure 4 shows a typical configuration where the LTMS is connected to the OBDH bus through a Data Bus Unit (DBU) and a Remote Bus Interface (RBI).

The CTMS is assumed to be integrated into the interrogation generator of the OBDH Central Data Management Unit (CDMU). To broadcast time information to all the LTMS components in the spacecraft, the CDMU modulates one of the BroadCast Pulse (BCP) bits transmitted in each 32 bit bus interrogation. This virtual serial line is coherent with the central elapsed time clock and has an effective bandwidth of one sixty-fourth of the bus bit rate, which is more than enough to carry the time messages, the synchronisation pulses and the phase references.

In the configuration shown, the LTMS operates in serial mode. To get the very highest resolution, the clock driving its ET counter is generated by a 16.77 MHz crystal directly connected to the built-in crystal oscillator cell. The internal DPLL adjusts this clock to the phase reference carried on the BCP output of the RBI. The synchronisation process between the LTMS and the CTMS is completely transparent to the application. Even after a complete reset of the application, no support from the processor is required since the LTMS will automatically synchronise its ET counter to the central time reference.

Previous implementations of time distribution have required extensive support from the application processor. One particular protocol required that the CDMU ordered each user to enable the time counter to be reset on reception of a broadcast pulse. This was performed by means of an OBDH bus interrogation. Next, the value of the central time reference at the reset instant was broadcast and had to be added to the local time counters by the application processor. As a last step, the users were ordered by an interrogation to disable further resets of the counter in question. It is clear that this protocol caused discontinuities in local time counters that could result in incorrect time information being provided to users. It also required a high level of involvement from the application processors to achieve time coherence throughout the spacecraft. The new standard protocol implemented by the LTMS relieves the application processor from such duties. It also avoids discontinuities in the local time counters and provides high resolution.

6 APPLIED DESIGN METHODOLOGY

The LTMS component has been developed using a top-down methodology based on VHDL simulation and synthesis. The LTMS was described on the behavioural level in VHDL and was verified extensively before the VHDL code was refined to allow synthesis.

The strict requirements on accurate timing lead to a design with several clock regions. Between each such region, the circuitry had to be carefully designed to minimise problems due to metastability. A detailed analysis of the synchronisation process and the related time facilities was performed. All delays that were identified to be caused by the circuitry introduced for metastability prevention have been compensated for.

A crystal oscillator cell was developed for the MITEL 1.25 µm CMOS/SOS5 standard cell library. The cell has been optimised for the nominal LTMS operating frequency of 16.77 MHz. This cell has been made generally available by the foundry to other users and is now part of the ASIC design kit.

Due to ET counter synchronisations only happening once a second and with clocking frequencies up to 16.77 MHz, the VHDL simulations had to use time skips to be able to verify the LTMS functionality within a reasonable time frame. These time skips had to be devised in such way that they did not upset the internal status of the LTMS or introduced timing violations. The serial nature of the CTMS messages resulted in long simulation runs. The programmability of the LTMS required several different test benches to be developed for complete verification. All simulation test benches had to be self-checking because a component with the complexity of the LTMS is impossible to check for functional correctness exclusively by visual inspection of the simulation results. The regression testing performed throughout the development also required the verification process to be automated.

Post-synthesis simulations were performed on a gate-level netlist expressed in the Verilog hardware description language. The VHDL test benches had to be adapted to generate the necessary Verilog stimuli.

Static timing verification after synthesis proved intricate because of the many clock regions and reset signals in the highly convoluted design. It was further complicated by the ongoing development of the MITEL 1.25 µm CMOS/SOS5 process which required the corresponding ASIC design kit, including the standard cell library, to be upgraded while in use.

A fault coverage greater than 98% for stuck-at faults has been reached by employing partial scan together with ad hoc methods and automatic scantest pattern generation. Functional test vectors have been developed allowing production testing of the LTMS to be performed at the nominal operating frequency of 16.77 MHz (and some additional margin).

The LTMS has a gate count of approximately 25 thousand equivalent gates and a die area of about 120 mm^2. It will be supplied in an 84 pin ceramic quad flat package. The LTMS will be guaranteed to withstand radiation up to a total dose of 100 kRad. It will be latch-up immune and will have a very low Single Event Upset (SEU) sensitivity due to the Silicon On Sapphire (SOS) technology.

7 CONCLUSIONS

A component which implements current and planned standards governing time distribution onboard spacecraft has been presented together with a potential application scenario. The LTMS components will supply their users with correctly phased, identical local copies of the central elapsed time reference onboard a spacecraft. The LTMS will detect and manage errors in the time distribution chain, and will provide its user with information regarding the validity of the local time reference. It will provide time stamping of events, an alarm clock, a stopwatch, waveform and pulse generators.

The development of the LTMS follows a design methodology using the hardware description languages VHDL and Verilog, together with automatic scan insertion and test pattern generation.

With the LTMS component, a novel way of time distribution with high resolution and accuracy has been introduced, requiring little or no support from the application incorporating it. The LTMS is currently being developed for the radiation hard SOS5 process from MITEL Semiconductors. First prototypes are expected in 2Q97.

Direct questions regarding price and availability of the LTMS to Mr Göran Wennergren at MITEL Semiconductors (Tel: +46 8 58024635).

8 ACKNOWLEDGEMENTS

We gratefully acknowledge Mr Damien Maeusli at the European Space Research and Technology Centre for the specification of the LTMS and for his valuable contributions to this paper.

9 ACRONYMS AND ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
BCP	BroadCast Pulse
CCSDS	Consultative Committee for Space Data Systems
CDMU	Central Data Management Unit
CMOS	Complementary Metal Oxide Semiconductor
CTMS	Central Time Management System
CUC	CCSDS Unsegmented Code
DBU	Data Bus Unit
DPLL	Digital Phase Locked Loop
ERC32	Embedded Real-time Computer
ERS	European Remote Sensing satellite
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
ET	Elapsed Time
IEEE	Institute of Electrical and Electronics Engineers
LTMS	Local Time Management System
OBDH	On-Board Data Handling
RBI	Remote Bus Interface
SEU	Single Event Upset
SOS	Silicon On Sapphire
VCA	Virtual Channel Assembler
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

10 REFERENCES

1 LTMS Preliminary Data Sheet, S. Redant et al., IMEC, October 1996.
2 Time Code Standards, Consultative Committee for Space Data Systems, CCSDS 301.0-B-2, Blue Book, Issue 2, April 1990.
3 4-255 Data Bus Protocol Extensions, PSS-04-256.