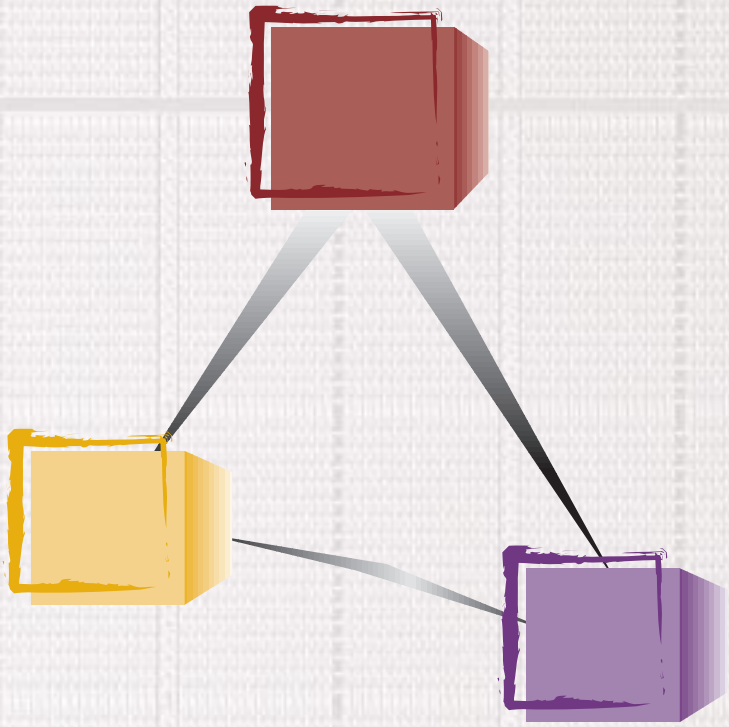
Actel's ProASIC Family

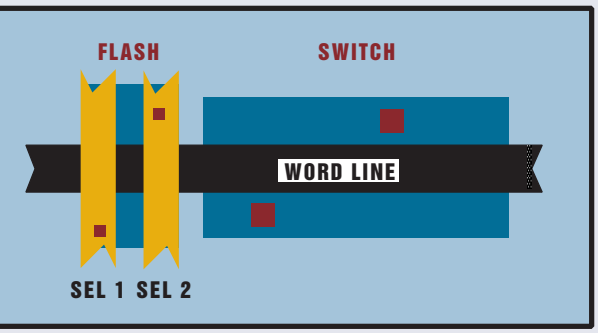
The Non-Volatile Reprogrammable Gate Array



Actel

The Flash Advantage

ProASIC Flash Switch



With densities ranging from 98,000 to 1 million gates, 200MHz system performance, and up to 130k bits of embedded two-port SRAM memory, Actel's ProASIC™ 500K family of programmable logic delivers high density programmable logic solutions. Based on a .25µ standard Flash process, ProASIC 500K devices combine high performance and low power with non-volatility and reprogrammability. Combining industry standard ASIC or FPGA design methodologies and tools with easy IP re-use and security, ProASIC 500K devices offer true reprogrammable system integration solutions.

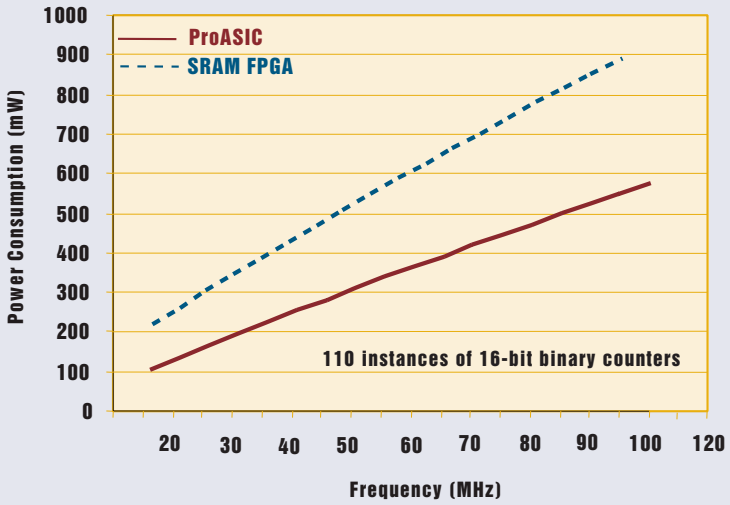
High Performance Architecture

Based on .25µ Flash technology that allows for performance enhancing architectural innovations, the small size of the Flash cell allows more programmable elements to be added into the routing, resulting in small routing segments. These segments offer predictable performance, improved utilization, and greater routing efficiency. The small Flash cell also allows the use of a very fine-grained logic, further improving logic utilization and predictability. The ProASIC 500K devices also offer the ability to fix pins at greater than 90% logic utilization, resulting in faster time-to-market. ProASIC 500K devices are the optimal programmable solution that allow designers to easily meet performance goals.

Low Power

Along with the high performance comes less power consumption. With the inherent efficiency of the routing structure and the architecture of the logic cell, ProASIC 500K devices consume 1/3 to 1/2 the power compared to SRAM based FPGAs. This lower power consumption results in a significant reduction in overall system cost.

ProASIC Power Consumption



Nonvolatile and Reprogrammable

Because the ProASIC 500K devices are nonvolatile, they retain their configuration almost indefinitely. This eliminates the cost of a boot PROM and the associated board space. Nonvolatile also means live on power up, so there is no period of nonfunctionality while configuration data is being downloaded from an external device. Additionally, ProASIC devices allow designers the flexibility to reprogram their devices if design changes are necessary.

IP Protection and Security

With the increasing complexity and density of devices, design security is a growing concern. ProASIC 500K devices offer an unprecedented level of design security. Without a startup bitstream, there is no possibility of the device's configuration data being intercepted. The devices also contain a read-protect security bit that prevents the programming content from being read out of the device. This read-protect bit cannot be cleared unless the entire device is erased. Finally, a unique licensing feature combined with factory programming ensures that the current business model for IP can now be extended to programmable technologies.

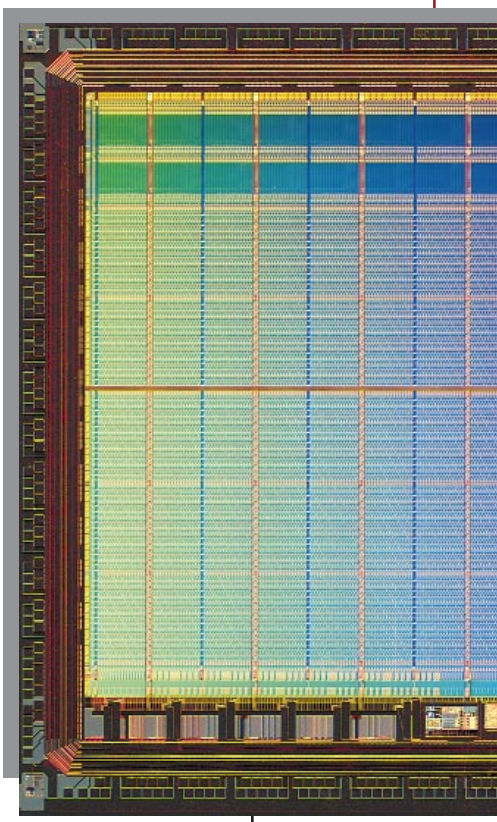
IP Re-Use

With increasing time-to-market pressures, designers do not have the luxury of developing every function from scratch. Design re-use is an important factor in meeting productivity goals. Due to the ProASIC 500K family's ASIC methodology and gate array-like architecture, bi-directional portability of functional blocks and commercially available IP is easily achieved.

ASIC and FPGA Design Flows

ProASIC devices work equally well with ASIC and FPGA methodologies. Designers who work in an FPGA design flow can take advantage of the ease of use and fast run times they have come to expect. ASIC designers will appreciate the high degree of control and easy integration into their existing design environment.

Because of the architecture, ProASIC 500K devices can use the same VHDL and Verilog HDL descriptions that are targeted for gate arrays and standard cells, freeing the designer from the limitations imposed upon HDL by some FPGA architectures. Additionally, standard ASIC tools are supported, protecting the designers' investment in tools and training while streamlining the design environment. As a result, the design team can focus on getting the design to market faster.

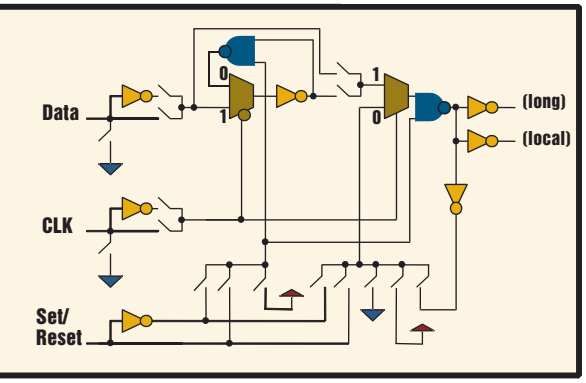


ProASIC 500K130 Die Actual Size

Flash Architecture

A Technology of Innovation

ProASIC Logic Tile



Compact Flash switches configure the chip functionality, the associated routing and clocking, and the underlying logic cell that provides the programmable gates. This switch consists of an NMOS transistor combined with a Flash memory cell and is controlled by a common floating gate, resulting in higher performance with lower power consumption.

Logic Tiles

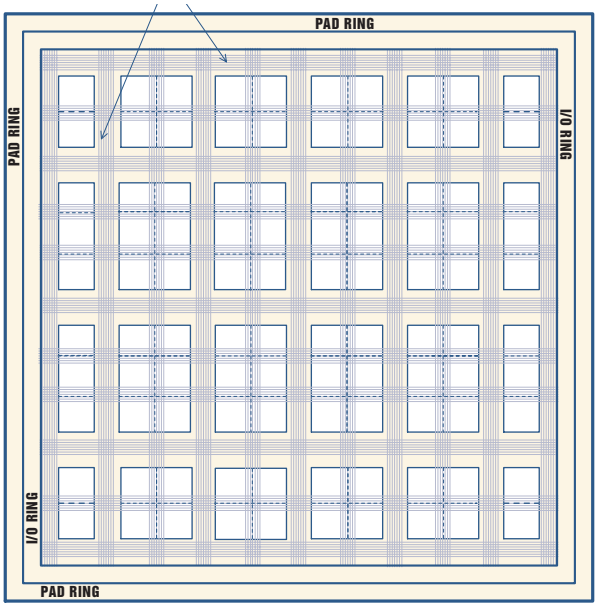
The small Flash switches makes it possible to utilize a fine-grained logic cell, resulting in better logic utilization. The basic logic unit consists of a programmable 3-input, 1-output cell. With the ability to program each input for signal inversion, the wasteful usage of cells as inverters is eliminated. Virtually any logic function can be programmed, including flip-flops. This provides a great deal of flexibility, allowing a programming range from 100% combinatorial to 100% sequential. Through the programming of the local switch matrix, the cell is configured and combined with adjacent cells to form larger logic functions. Similar to a sea-of-gates gate array architecture, the basic logic tiles are stepped and repeated in the horizontal and vertical directions to create a programmable Sea-of-Tiles.™

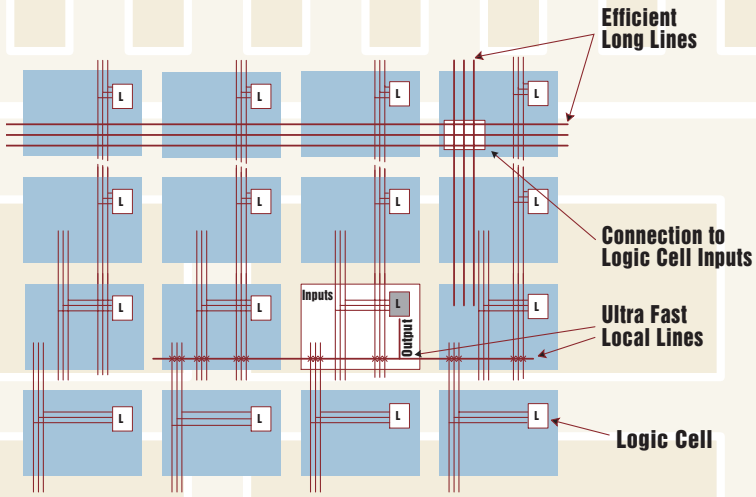
Routing Resources

The interconnect routing resources are organized in four hierarchical levels, providing high performance with routing flexibility. This hierarchical routing structure provides optimal place and route solutions for varying design styles and application types. The four levels of routing networks are as follows:

- Ultra Fast Local resources are high speed dedicated lines that allow a direct connection from the output of every tile to I/O buffers, memory blocks, or the eight surrounding tiles.
- Efficient Long Line resources vary in length from 1, 2, or 4 tiles and provide routing for greater distance and higher fanout connections.
- High Speed Bus resources run vertically and horizontally across a chip. They are able to travel across the chip with minimal delay and can be used for busses, datapath functions, or very high fanout nets.
- High Performance Global networks are used to distribute clocks, resets, and other nets requiring high fanout with minimal delay or skew.

High Speed Bus Resources





Ultra Fast Local and Efficient Long Line Resources

Embedded Two-Port SRAM

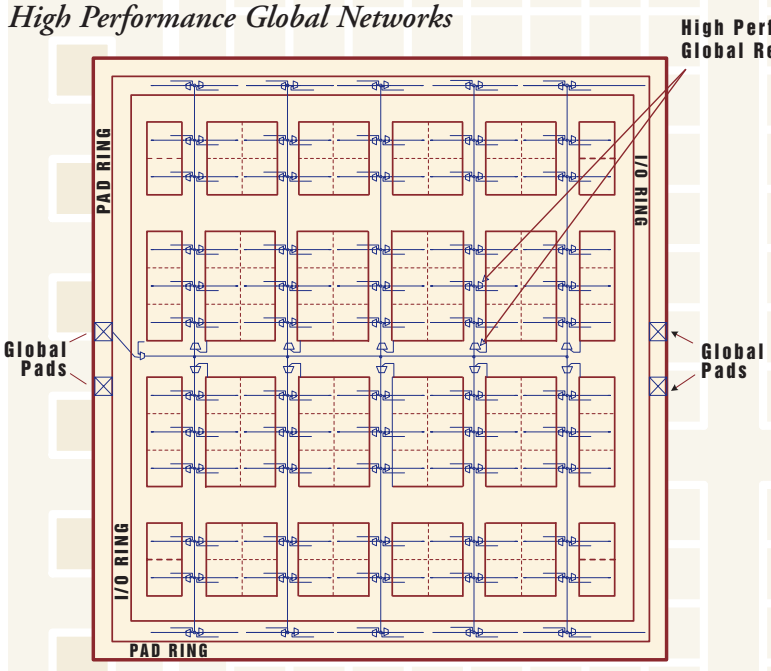
As chip densities increase, embedded and dedicated memories become essential. The ProASIC 500K devices provide up to 130k bits of embedded two-port memory. Depending on the device, available memory ranges from 6 to 60 blocks that can support a variety of possible memory configurations. Each block contains a 256 word deep by 9-bit wide memory. With every block, there is the option to program it as an independent memory, or combine it with other blocks to form larger, more complex memories. Each memory block can be configured as synchronous or asynchronous, FIFO or SRAM, and single port or multiport. In addition, the memory blocks include hardwired decoder, I/O circuits, parity generation and detection circuits, FIFO flag generation logic, and timing and control circuits to minimize external logic gate count and complexity.

Programmable I/Os

The ProASIC 500K devices provide fully configurable I/Os for greater flexibility and performance. Each pad can be programmed as an input, an output, a three-state driver, or a bi-directional buffer.

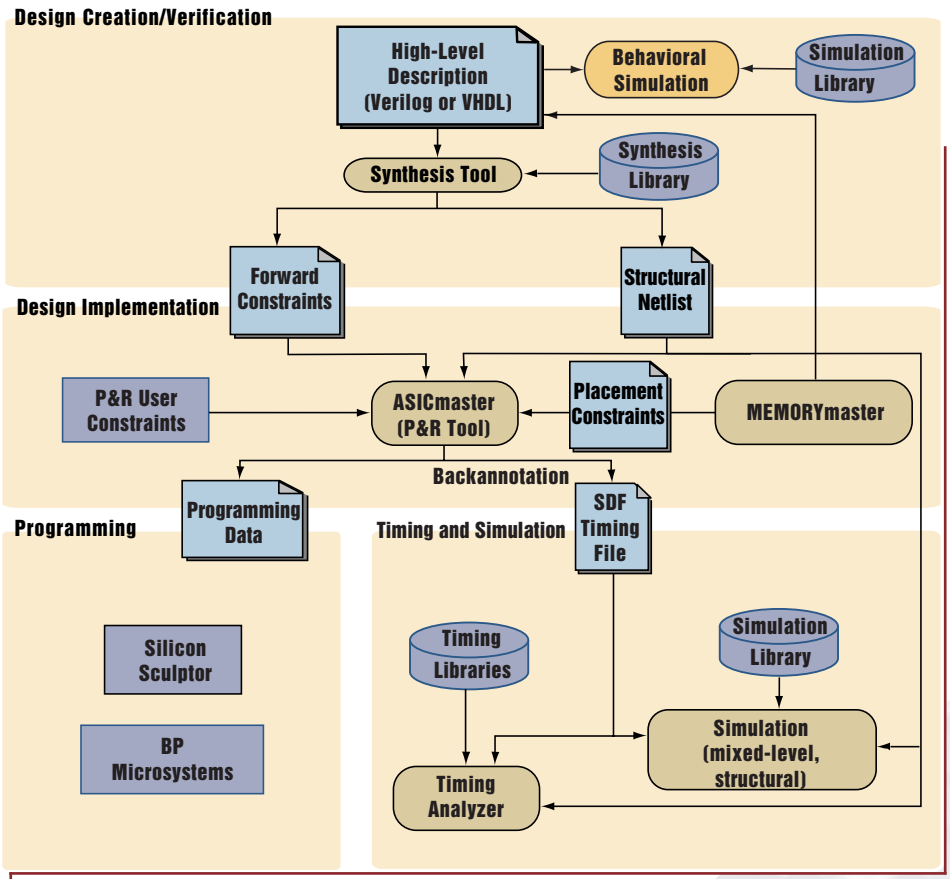
Additional programming options include pull-up resistors and selectable drive and slew rates that enable close matching to a wide range of bus interface conditions. The cells are programmed for LVCMOS or 3.3V PCI interface specifications. ProASIC 500K devices provide the capability to individually select each input/output device to interface with either 2.5V or 3.3V components.

High Performance Global Networks



Design Tools

Actel's ProASIC 500K devices are supported by ASICmaster™ and MEMORYmaster™ software, as well as third party CAE tools, offering designers an open design environment. ProASIC devices work equally well in ASIC and FPGA design environments, allowing designers to leverage their existing design tools.



ASICmaster

ASICmaster is an automatic place and route tool that runs on Sun® and HP® workstations, as well as on Windows® NT™. ASICmaster accepts standard ASIC formatted netlists and performs timing-driven place and route. Incremental place and route is supported for ASIC-like ECO (Engineering Change Notice) capability. ASICmaster can be used as a push button tool, or the designers can interactively control the place and route process. ASICmaster also includes a power estimator and provides back annotated delay information for simulation or static timing analysis.

MEMORYmaster

MEMORYmaster is a tool that automatically generates memories from inputs given by the designer. The designer has the ability to select the depth and width, synchronous or asynchronous functionality of the ports, and usage of parity generation or check. If it is a synchronous read port, the designer can choose whether the output is pipelined or transparent. MEMORYmaster also generates simulation models and a constraints file that contains placement information for created memory.

Third Party Support

	Synthesis	Simulation	Static Timing
Synopsys	Design Compiler FPGA Express*	VSS	Prime Time
Cadence	BuildGates	Verilog-XL	
Exemplar	Leonardo Spectrum*		
Model Techology		ModelSim	

* Q3 99

Silicon Sculptor

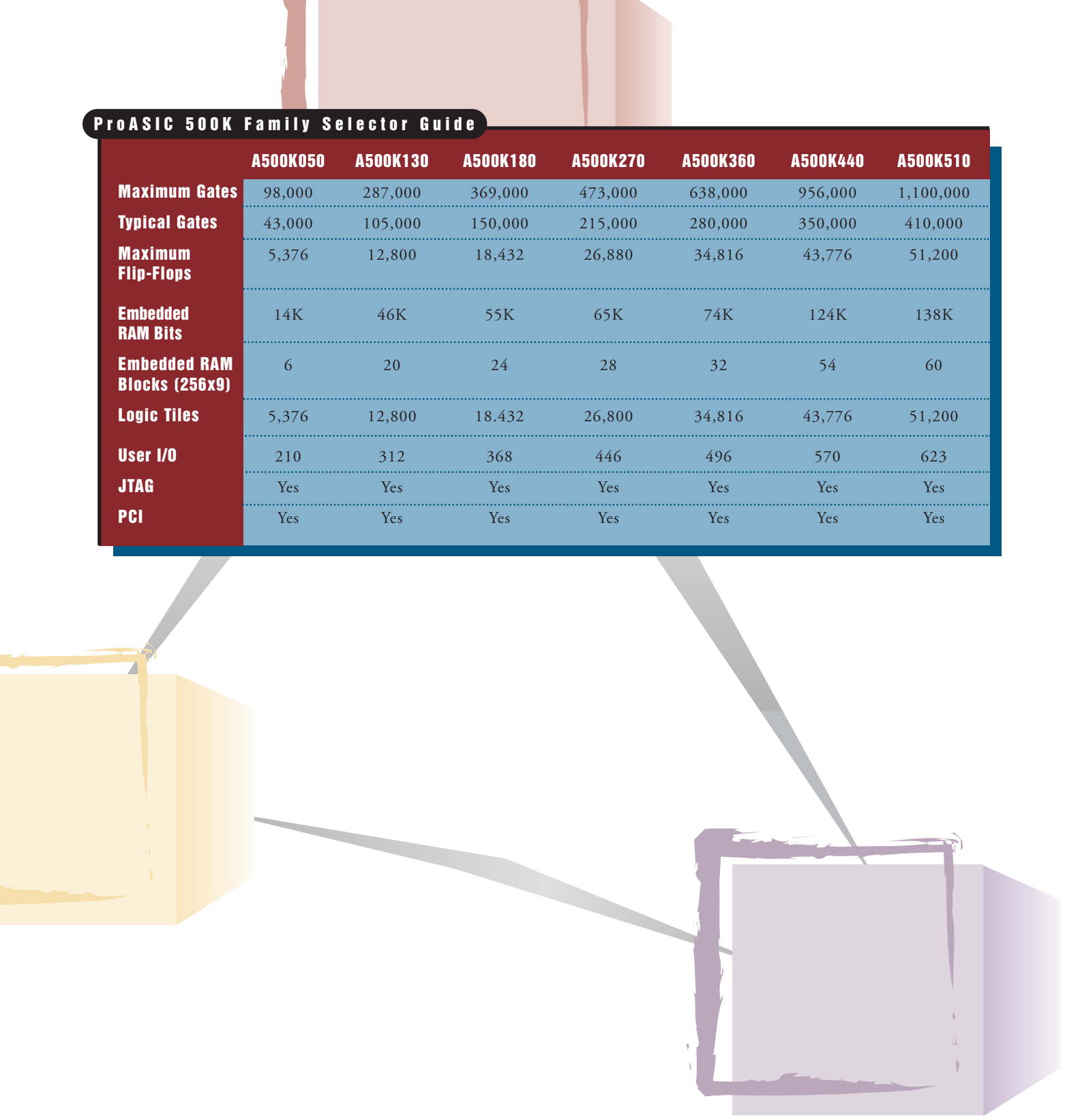
ProASIC 500K devices have in-system programming capabilities using Actel's Silicon Sculptor. To program a device, the configuration data is supplied through a standard JTAG interface. Silicon Sculptor is a concurrent programmer that allows multiple sites to operate independently and enables the concurrent programming of multiple devices, speeding high volume production programming. The upcoming Silicon Explorer II will also provide programming support.

Protocol Design Services

Actel's *Protocol* Design Services team has a ten-year history of providing hardware and software design services and offers its customers varying levels of design support at any stage of product development. The level of project involvement is customer-driven, ranging from full design service to custom solutions. With over 1000 designs, including 50 ProASIC designs, *Protocol* Design Services has significant experience prototyping and designing ProASIC devices. The management team offers design expertise, the ability to quickly adapt to changing design environments and project requirements, and a commitment to delivering services on time, within budget, and to the customers' specifications.

ProASIC 500K Family Selector Guide

	A500K050	A500K130	A500K180	A500K270	A500K360	A500K440	A500K510
Maximum Gates	98,000	287,000	369,000	473,000	638,000	956,000	1,100,000
Typical Gates	43,000	105,000	150,000	215,000	280,000	350,000	410,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Embedded RAM Bits	14K	46K	55K	65K	74K	124K	138K
Embedded RAM Blocks (256x9)	6	20	24	28	32	54	60
Logic Tiles	5,376	12,800	18.432	26,800	34,816	43,776	51,200
User I/O	210	312	368	446	496	570	623
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes



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