Power-Up Device Behavior of Actel FPGAs

Introduction

In Actel's antifuse FPGAs, the user programmable link between horizontal and vertical routing tracks is permanent, and therefore similar to that of an ASIC, which is programmed at the mask level with a via. The permanent, nature of the link has proven to be highly desirable in many applications, such as HiRel satellite command and control applications or control logic on hot-swappable telecom switches. However, even though the links are similar, Actel's antifuse FPGAs do not behave in the same way as ASICs during the power-up period. This results from the routing tracks being connected to the logic modules through a pass transistor that is controlled by a charge-pump voltage. During programming, the pump is off, and the logic modules are isolated from the tracks being programmed. During normal operation, the sequence in which the pump is turned on and the tracks are connected to the logic module during power up determines the behavior of the device during power up. The sequence has been improved over time, resulting in different antifuse FPGA families exhibiting different power-up behaviors. This application note summarizes the power-up behavior of Actel FPGAs.

Power-Up Behavior of Actel Antifuse FPGAs

The power-up sequence of a design affects two aspects of power-up behavior, I/O behavior and transient current behavior. These power-up conditions concern the system designer because they affect the delay until the device reaches full functionality.

During power up, the supply rail of a system typically has a linear rise with a slope in the range of 0.1V/ms to 5V/ms. The behavior of some of the families when powered up in this range is different from when they are powered up quickly (0.5V/µs). When there is a difference in behavior, it will be noted.

I/O Behavior

Actel's newest antifuse FPGAs are designed with circuitry that forces all of the I/Os into the high-impedance tristate mode during power up before the device becomes functional. However, for the original Legacy antifuse FPGA families, the I/Os, regardless of whether they are programmed to be inputs, outputs, bibufs or tribufs during operation, can temporarily behave as outputs during power up. This behavior varies with the speed at which power is applied to the device. It occurs during a 0.3V window in a slow power-up ramp (typically tested at 0.2V/ms) when V_{CC} is between 1.0V and 2.5V. None of the families exhibit this behavior during fast power up (tested at 0.5V/µs), and the I/Os remain tristated until the device functions as programmed.

Table 1 on page 2 summarizes the behavior of the I/Os during power up for several Actel antifuse FPGA families.

Transient Current Surge

During the power-up ramp, there is typically a period of relatively high transient current (I_{CC}). This transient current occurs when the pump is enabled and all of the logic modules are simultaneously connected to the routing tracks. The transient current begins when V_{CC} reaches 1.5V to 2.0V, but its duration depends on the V_{CC} ramp rate. In all cases, the transient current occurs 250µs after operating V_{CC} is reached. Table 2 on page 2 summarizes transient current behavior during power up.

Table 1 • I/O Behavior during Power Up

Family	Slow Power Up (0.2V/ms)	Fast Power Up (0.5V/μs)
ACT 1/RH1020	Behave as outputs driving either high or low for up to 5 ms.	Tristate
ACT 2/RH1280 1200XL, 3200DX	Behave as outputs driving high for less than 1ms.	Tristate
ACT 3	Tristate	Tristate
RTSX	Tristate	Tristate
42MX	Tristate	Non X-39 devices will go to an unknown state, causing functional failure.
SX-A	Tristate	Tristate
RTSX-S	Tristate	Tristate
eX	Tristate	Tristate

Note: For information on other Actel devices, contact your Actel representative.

Table 2 • Transient Current Behavior during Power Up

Family	Transient Current (mA)	Comments
ACT 1/RH1020	10–60	
ACT 2/RH1280 1200XL, 3200DX	10–50	
ACT 3	10–60	
RTSX	400	V_{CCR} powered to 5.0V and V_{CCI}/V_{CCA} powered to 3.3V. Behavior is independent of the power-up sequence. The transient current is in the V_{CCA} rail.
42MX	90-539	Depends on the operating voltage (3.3V or 5.0V). For non X-39 devices, it is slightly higher.
SX-A	45-557	Depends on the ramp on V_{CCA} rail.
RTSX-S	144-790	Depends on the ramp on V_{CCA} rail.
eX	N/A	

Note: For information on other Actel devices, contact your Actel representative.

Conclusion

A device is considered functional once the inputs and outputs behave as expected by the designer. The exact moment a device becomes functional is dependent on the FPGA family and the ramp rate of V_{CC}. However, in all cases, the device is functional within 250μs after nominal V_{CC} is reached, regardless of family or ramp rate.

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