# Axcelerator Family FPGAs

FuseLock™

## Leading-Edge Performance

- 350+ MHz System Performance
- 500+ MHZ Internal Performance
- High-Performance Embedded FIFOs
- 700Mb/s LVDS Capable I/Os

## Specifications

- Up to 2 Million Equivalent System Gates
- Up to 684 I/Os
- Up to 10,752 Dedicated Flip-Flops
- Up to 339kbits Embedded SRAM/FIFO
- Manufactured on Advanced 0.15µm CMOS Antifuse Process Technology, 7 Layers of Metal

## Features

- Single-Chip, Nonvolatile Solution
- Up to 100% Resource Utilization with 100% Pin Locking
- 1.5V Core Voltage for Low Power
- Footprint Compatible Packaging
- Flexible, Multi-Standard I/Os:
  - 1.5V, 1.8V, 2.5V, 3.3V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS, 3.3V PCI, and 3.3V PCI-X
  - Differential I/O Standards: LVPECL and LVDS
  - Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
  - Registered I/Os with 64-bit deep FIFO on Each Pin ("PerPin FIFO")
  - Hot-Swap Compliant I/Os (Except PCI)
  - Programmable Slew Rate and Drive Strength on Outputs
  - Programmable Delay and Weak Pull-Up/Pull-Down Circuits on Inputs
- Embedded Memory:
  - Variable-Aspect 4,608-bit RAM Blocks (x1, x2, x4, x9, x18, x36 Organizations Available)
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
  - ROM Emulation Capability
- Segmentable Clock Resources
- Embedded Phase-Locked Loop:
  - 14-200 MHz Input Range
  - Frequency Synthesis Capabilities up to 1 GHz
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability with Actel Silicon Explorer II
- Boundary-Scan Testing Compliant with IEEE Standard 1149.1 (JTAG)
- FuseLock™ Secure Programming Technology Prevents Reverse Engineering and Design Theft

## Axcelerator Family Product Profile

| Device | AX125 | AX250 | AX500 | AX1000 | AX2000 |
|---|---|---|---|---|---|
| **Capacity (in Equivalent System Gates)** | 125,000 | 250,000 | 500,000 | 1,000,000 | 2,000,000 |
| Typical Gates | 82,000 | 154,000 | 286,000 | 612,000 | 1,060,000 |
| **Modules** | | | | | |
| Register (R-cells) | 672 | 1,408 | 2,688 | 6,048 | 10,752 |
| Combinatorial (C-cells) | 1,344 | 2,816 | 5,376 | 12,096 | 21,504 |
| Maximum Flip-Flops | 1,344 | 2,816 | 5,376 | 12,096 | 21,504 |
| **Embedded RAM/FIFO** | | | | | |
| Number of Core RAM Blocks | 4 | 12 | 16 | 36 | 64 |
| Total Bits of Core RAM | 18,432 | 55,296 | 73,728 | 165,888 | 294,912 |
| Number of PerPin FIFOs | 168 | 248 | 336 | 516 | 684 |
| Total PerPin FIFO Bits | 10,752 | 15,872 | 21,504 | 33,024 | 43,776 |
| Total Embedded RAM Bits | 29,184 | 71,168 | 95,232 | 198,912 | 338,688 |
| **Clocks (Segmentable)** | | | | | |
| Hardwired | 4 | 4 | 4 | 4 | 4 |
| Routed | 4 | 4 | 4 | 4 | 4 |
| **PLLs** | 8 | 8 | 8 | 8 | 8 |
| **I/Os** | | | | | |
| I/O Banks | 8 | 8 | 8 | 8 | 8 |
| I/O Blocks | 8 | 16 | 16 | 24 | 32 |
| Maximum User I/Os | 168 | 248 | 336 | 516 | 684 |
| Maximum LVDS Channels | 84 | 124 | 168 | 258 | 342 |
| Total I/O Registers | 504 | 744 | 1,008 | 1,548 | 2,052 |
| **Package** | | | | | |
| CSP | 180 | | | | |
| BGA | | | | 729 | |
| FBGA | 256, 324 | 256, 484 | 484, 676 | 484, 676, 896 | 896, 1152 |

## General Description

Actel's newest FPGA family, Axcelerator offers high performance at densities of up to two million equivalent system gates. Based upon Actel's new AX architecture, Axcelerator has several system level features such as embedded SRAM (with complete FIFO control logic), PLLs, Segmentable Clocks, chip-wide highway routing, and PerPin FIFOs.

### Device Architecture

Actel's AX architecture, derived from the highly successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1). There are two base logic modules: the Register Cell (R-cell), containing a full-featured flip-flop and the Combinatorial Cell (C-cell), containing a four-input MUX with control and carry-chain logic.

Two C-cells and a single R-cell form a Cluster, and two Clusters comprise a SuperCluster. SuperClusters are organized into Core Tiles, which are combined to generate each device (please refer to the *Axcelerator Family FPGAs* data sheet for more information).

Additionally, each SuperCluster contains an independent Buffer Module. Buffer Modules support automatic buffer insertion for high-fanout nets by the place-and-route tool, providing better overall system delays while improving logic utilization.

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

### Embedded Memory

The embedded, variable-aspect-ratio SRAM blocks have separate read and write ports that can be configured with different bit widths on each port. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bit. Additionally, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO, with programmable DEPTH and programmable ALMOST-EMPTY and ALMOST-FULL flags in addition to the normal FULL and EMPTY flags.

The embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as metastable control circuitry to prevent erroneous operation. The metastable control circuitry, when combined with the FIFO's ability for asynchronous reads and writes, enables these embedded structures to be used to cross both clock and phase domains.

### I/Os

The Axcelerator family of FPGAs also features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/O: 1.5V, 1.8V, 2.5V and 3.3V. In total, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). All I/O options are 3.3V tolerant; the 3.3V PCI option is 5V tolerant with the aid of an external resistor. All I/O options except 3.3V PCI are hot-insertion capable.

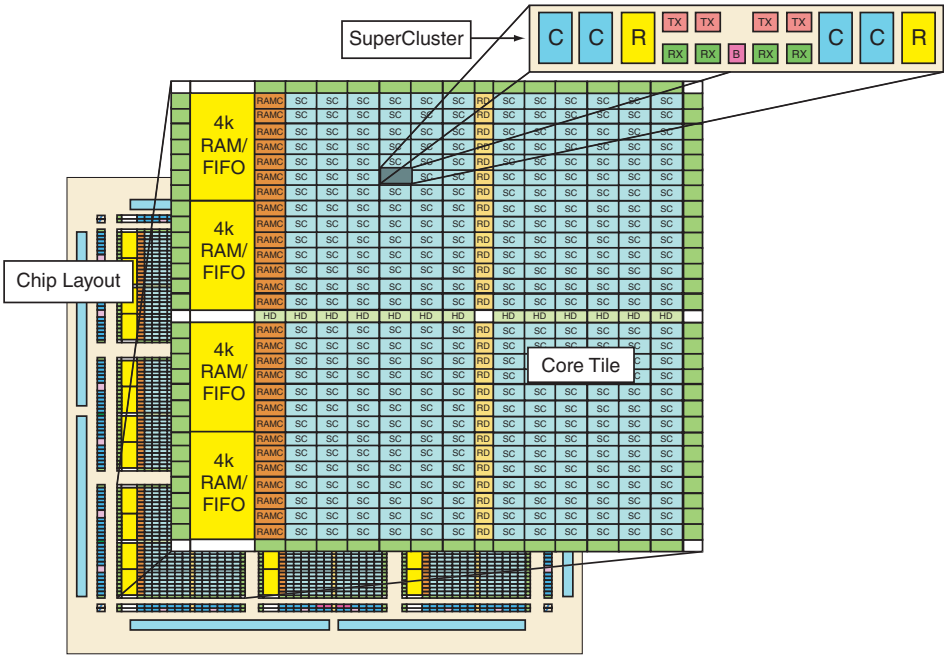


***Figure 1 •*** *AX Device Architecture*

Each I/O has an input, output, and enable register. Unique to the AX architecture is a 64-bit PerPin I/O FIFO, enabling buffering of either input or output data. The PerPin FIFO can be bypassed if desired. The I/O FIFO Embedded Controller can be used to provide clocking, ALMOST-EMPTY, ALMOST-FULL, FULL and EMPTY flags. Each PerPin FIFO can be individually controlled by internal logic.

### Routing

Tying all of the device resources together is the AX hierarchical routing structure, enabling the Axcelerator family's high performance and utilization. At the lowest level in and between SuperClusters, there are three routing structures: DirectConnects, FastConnects, and CarryConnects. DirectConnects provide very high performance routing inside the SuperCluster, while FastConnects provide high performance routing inside the SuperCluster and to the below SuperCluster. CarryConnect routing is used between SuperClusters when building arithmetic functions. The core tile routing is at the next level. Both vertical and horizontal tracks run across a row or column of SuperClusters within a core tile respectively. At the chip level, routing highways extend across the full length of the device, both north-to-south and east-to-west.

### Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLKs) per device, which can directly drive the clock input of an R-Cell. Each of the four routed clocks (CLKs) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell. Global clear (GCLR) and global preset (GPSET) can drive the clear and preset inputs of each R-Cell as well as each I/O Register on a chip-wide basis at power up.

Each HCLK and CLK has an associated analog PLL for a total of eight per chip. Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL can operate with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by up to a factor of 64, or multiply and divide settings can be in any combination as long as the resulting clock does not exceed the absolute maximum output value (1 GHz).

Additionally, the PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock needed to drive the PLL can be derived from three sources: an external input pad (configured as either single-ended or differential), internal logic, or from the output of an adjacent PLL.

## Summary

Actel's Axcelerator family of FPGAs expands the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, high-speed I/Os, and PerPin FIFOs. The Axcelerator family also provides the designer with high-performance at high-gate counts with high device utilization even with fixed pins.

## Product Plan

| | Speed Grade | | | | Application | |
|---|---|---|---|---|---|---|
| | Std | –1 | –2 | –3 | C | I |
| **AX125 Device** | | | | | | |
| 180-Pin Chip Scale Package (CSP) | P | P | P | P | P | P |
| 256-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 324-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| **AX250 Device** | | | | | | |
| 256-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 484-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| **AX500 Device** | | | | | | |
| 484-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 676-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| **AX1000 Device** | | | | | | |
| 484-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 676-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 729-Pin Ball Grid Array (BGA) | P | P | P | P | P | P |
| 896-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| **AX2000 Device** | | | | | | |
| 896-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |
| 1152-Pin Fine Ball Grid Array (FBGA) | P | P | P | P | P | P |

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*Applications:* *C = Commercial* *I = Industrial*

*Availability:* ✔ = *Limited Availability. Contact your Actel Sales representative for the latest availability information.* *P = Planned*

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as “Product Brief,” “Advanced,” “Production,” and “Web-only.” The definition of these categories are as follows:

### Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.



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